Strain Engineered $In_xGa_{1-x}As$ Channel pHEMTs on Virtual Substrates: A Simulation Study

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The impact of $In_xAl_{1-x}As$ strain control buffers on the performance of low In content InGaAs channel pseudomorphic high electron mobility transistor (pHEMT) is investigated. It is shown that relaxed and tensile strained channel devices outperform the conventional compressively strained channel devices. It is argued that strain engineering in GaAs based devices makes it possible to realise RF characteristics comparable to InP based pHEMTs while obtaining improved breakdown characteristics.

1. Introduction

Pseudomorphic High Electron Mobility Transistors (pHEMTs) with compressively strained $In_xGa_{1-x}As$ channels ($x<0.3$) grown on GaAs substrates are widely used in commercial MMIC applications [1]. The mainstream research now is focused on devices with higher In content channels, lattice matched to InP substrates ($x=0.53$), or compressively strained ($x>0.53$) channels grown on InP substrates [2]. The increased In content reduces the Γ-valley effective mass and increases the Γ-L separation and the conduction band offset, resulting in higher mobility, greater velocity overshoot, increased carrier density and confinement, and overall improvement in the device performance [3]. There are, however, drawbacks. The reduction of the bandgap in In rich channels increases the impact ionisation leading to kink effects and premature breakdown [4]. Handling the fragile InP substrate presents additional technological problems. An alternative approach is to use 'virtual substrates' where relaxed InAlAs buffers are grown on conventional GaAs wafers to match various channel lattice constants [5].

In this paper we study the possibility of using strain engineering to enhance the performance of HEMTs with low In content $In_xGa_{1-x}As$ channels grown on virtual GaAs substrates, thus avoiding the detrimental effects associated with the impact ionisation in In rich devices. We study the high field transport properties and overshoot effects in channels under various strain conditions.

The layer structure and the architecture of the devices under consideration are described in Section 3. The high field transport results and the corresponding impact on the real device performance are presented in Section 4. We also compare the important figures of merit for relaxed and strained channel devices. The conclusions are drawn in Section 5.

2. Strain Engineering

The concept of channel strain engineering can be realised in HEMT design through the use of InAlAs buffers, with different In compositions, as virtual substrates. The induced strain alters the transport properties and controls device performance even without changing the InGaAs channel composition. The compressive strain in conventional GaAs and InP pseudomorphic HEMTs lowers the symmetry of the crystal lattice transforming the spherical Γ-valley minima into an ellipsoidal valley. The effective mass components parallel and perpendicular to the strain plane, $m_{\|comp}$ and $m_{\perp comp}$ respectively, are both larger than the effective mass in the relaxed case [6]

$$m_{relax} < m_{\|comp} < m_{\perp comp} \tag{1}$$

The six-fold degenerate X-valleys are split into a four-fold quadruplet and a two fold pair. There is experimental evidence to show that reduction of the compressive strain increases the low field mobility in InGaAs channels [7]. The introduction of tensile strain may further improve the channel transport properties compared to the relaxed case. Under tensile strain conditions, the effective masses parallel and normal to the interface both become lower than the relaxed effective mass:

$$m_{relax} > m_{\|tens} > m_{\perp tens}. \tag{2}$$

At the same time, however, the bandgap decreases with the increasing strain:

$$E_g^{comp} > E_g^{relax} > E_g^{tens}. \tag{3}$$

Monte Carlo simulations have shown that the low field mobility increases rapidly with the increasing tensile strain

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[6]. However, no high field simulations of overshoot effects in tensile strained channels have been reported.

In this study we explore the performance potential of relaxed and tensile strained, low In content InGaAs channel pHEMTs. The simulations are calibrated with respect to dc and RF measurements of a real 120nm HEMT with a compressively strained channel grown on GaAs substrate. This device is fabricated at the Glasgow Nanoelectronics Research Centre.

3. Methodology and device architecture

In this study we use the Monte-Carlo module of the simulator H2F [8]. It utilises quadrilateral finite elements to describe the geometry of recessed compound FETs. H2F takes into account the effects related to the geometry of the gate and recess region and surface effects. The characteristics of the simulated devices are investigated using the Monte Carlo RF analysis technique described in [9]. A methodology has been developed to include the effect of the parasitic series resistances introduced by the contacts and the connection pads on the dc device characteristics [10]. This allows accurate calibration against measured dc characteristics of fabricated devices.

The RF analysis is carried out using transient Monte Carlo simulations [9]. For a given operating point the steady-state condition is first established. A small step change is then applied to the gate/drain voltages and the traces of the gate and drain currents are recorded. The Ramo-Shockley formalism is implemented to reduce the noise in the transient terminal currents. The frequency dependent small signal y-parameters of the simulated device are extracted by Fourier transforming the transient traces. The cut-off frequency f_T is estimated from the y-parameters whereas the maximum frequency of oscillation, f_{max}, is estimated after transforming the y-parameters into s-parameters. The equivalent circuit parameters are calculated analytically from the y-parameters [11]. The corresponding figures of merit for a 'real' device are extracted by incorporating the parasitic equivalent circuit components, not present in the Monte Carlo simulations, into the y- and s-parameters extracted from the transient simulation. The noise characteristics can also be estimated from the stochastic nature of the steady-state Monte Carlo current and the small signal parameters.

The scattering mechanisms employed include ionised and neutral impurity, piezoelectric, acoustic phonon, polar optic phonon and non-polar scattering mechanisms. For the transient simulations, time steps of Δt = 0.125-1.000 fs are used so that the beginning of the transient is properly resolved. The different strain-dependent parameters for the InGaAs channel were chosen from [3 & 6].

We investigate the performance of low In content channel pseudomorphic HEMT devices based on the Glasgow University device design. The benchmark in this investigation is a 120nm gate-length $In_{0.3}Ga_{0.7}As$ channel pHEMT structure, Fig.1(A). It comprises a 100 period superlattice grown on s.i. GaAs substrate followed by a 600nm GaAs buffer. The strained $In_{0.3}Ga_{0.7}As$ channel is 10nm thick and is separated from the Si δ-doping by a relatively thin (2.5nm) $Al_{0.3}Ga_{0.7}As$ spacer. The N_s=5x10^{12}cm^{-2} effective δ-doping is encapsulated between 3 and 2 monolayers of GaAs. A 12.5nm $Al_{0.3}Ga_{0.7}As$ Schottky layer, and 5nm $Al_{0.3}Ga_{0.7}As$ recess etch stopper are grown on top of the δ-doping. The overall separation between the channel and the gate is 21.5nm. A 30nm *heavily doped* (N_d=4x10^{18}cm^{-3}) GaAs cap layer screens the 2DEG in the region between the gate and the contacts from the negative charge of electrons trapped on deep, acceptor type surface states. The gate length is 120nm with 50nm gate recess on each side of the gate. The device has a channel width of 100μm. The separation between the source and the drain contacts is 1μm.

The in-plane built-in strain is due to the lattice misfit between the 10nm wide $In_{0.3}Ga_{0.7}As$ channel and the thick GaAs substrate. Experimental [5] and theoretical [3,6] evidence suggest that the performance of such devices may be improved by full or partial relaxation of the channel strain. The relative values of the lattice constants of III-V materials indicate that channel relaxation may be achieved by using thick InAlAs as a strain-relief buffer or a virtual substrate. Not only can this buffer help relax the InGaAs channel, it can alternatively allow a tensile strain to be achieved.

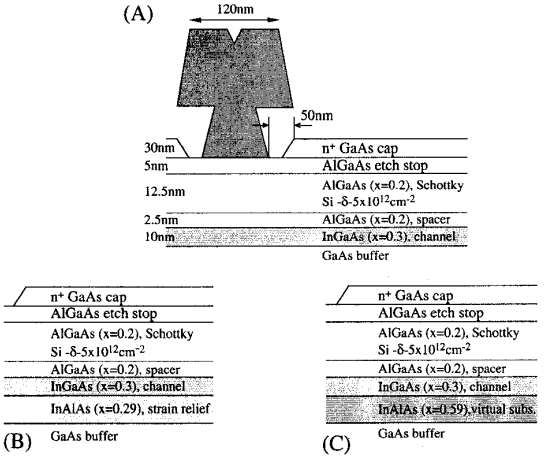

Figure 1: Structures of the devices with the channel being under: (A) compressive strain, (B) relaxed & (C) tensile strain.

For an $In_{0.3}Ga_{0.7}As$ channel grown on $In_xAl_{1-x}As$ virtual substrate, the in-plane built-in strain can be expressed in terms of the In content as:

$$e_{\parallel} = 0.06893x - 0.01974 \qquad (4)$$

It is clear that both compressive ($e_{\parallel} < 0$) and tensile ($e_{\parallel} > 0$) strain types could be realised by controlling the In content of the virtual substrate. It is therefore possible to achieve strain relaxation in the channel resulting in a lattice match using $In_{0.28}Al_{0.72}As$, device B, Fig.1(B). The strain relief advantage is also accompanied by a large improvement

in the conduction band offset between the channel and the substrate which increases to about 1eV.

The compressive strain built in the channel of the reference device, A, is 0.021. A strain of the same magnitude but of a tensile nature can be achieved through the use of the virtual substrate $In_{0.59}Al_{0.41}As$ referred to as device C, Fig.1(C). The conduction band offset between the channel and the virtual substrate is about 0.2eV, less than the band offset of device A (0.3eV). The layer structure above the channel of both devices B & C is kept identical to that of the benchmark device, A.

4. Results and discussion

First we examine the uniform high field transport properties in $In_{0.3}Ga_{0.7}As$ material under compressive, relaxed and tensile strain conditions corresponding to devices A, B and C.

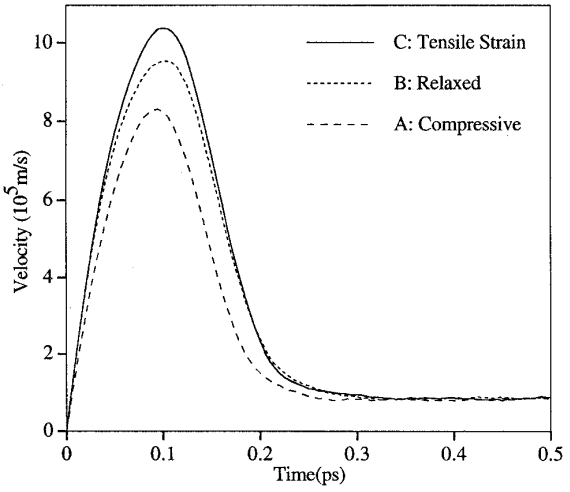

Figure 2: Evolution of average velocity in $In_{0.3}Ga_{0.7}As$ following the application of an electric field of 60kV/cm.

The simulations have shown that the spatial and temporal velocity overshoot profiles are significantly affected by the strain conditions. Fig.2 illustrates the temporal evolution of the velocity of electrons following the application of an electric field E=60kV/cm. The maximum velocity attainable increases by 25% as the strain conditions are varied from compressive to tensile strain. The time it takes the electrons to attain the maximum value is slightly longer in the tensile strain case. Particularly pronounced is the increased overshoot in the case of tensile strain. The steady-state saturation velocity remains relatively unaffected by the strain variations. The significant velocity overshoot in relaxed and tensile strained channels together with the low field mobility enhancement promise a significant performance enhancement in the corresponding HEMTs.

The average velocities along the channel of the three 120nm gate length pHEMTs are compared in Fig.3 for compressive (device A), relaxed (device B) and tensile (device C) strain conditions (V_D=1.5V & V_G=0V). The maximum velocity increases by about 60% as the strain changes sign from compressive to tensile strain. The corresponding overshoot extends over a longer distance in the channel region between the gate and the drain. The position of the maximum velocity shifts towards the drain. It is, however, the increase in the velocity near the source end of the channel which dominates the increase in total current in relaxed and, more significantly, in tensile strain conditions.

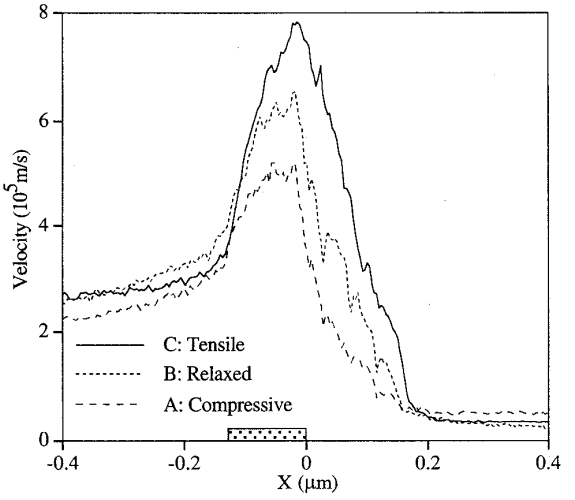

Figure 3: Velocity profile in the channel of 120nm gate-length HEMTs, V_D=1.5V & V_G=0V.

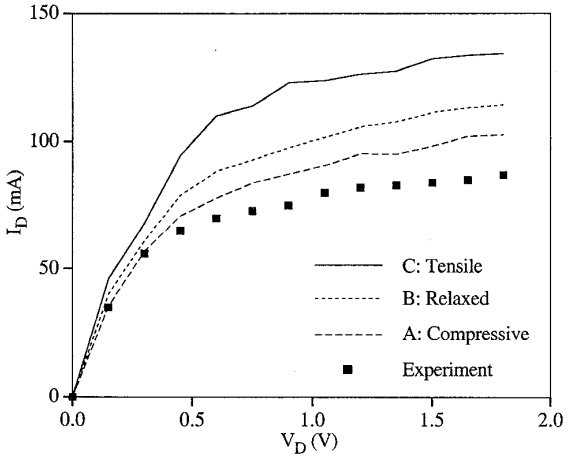

Figure 4: I_D-V_D characteristics of the pHEMTs at V_G=0V.

Fig.4 shows a comparison between the I_D-V_D characteristics for the relaxed, compressively strained and tensile strained channel conditions calculated at V_G=0V. The results shown in Fig.4 incorporate the effects of the gate, source and drain contact resistances which are excluded from the Monte Carlo simulations [10]. It is clear that there is a significant increase in the drain current as a result of the change in strain conditions. The drain current device A is about 10% lower than the current under relaxed conditions,

device B. Furthermore, the drain current under tensile strain conditions, device C, is found to be 18% higher than the current in B. This increase is brought about by the significant increase in the channel velocity at the source end of the transistor and the large increase in the velocity overshoot under the channel.

	Tensile (C)	Relaxed (B)	Comp. (A)	Experiment
C_{gs} (fF)	76	75.7	68	77.8
C_{gd} (fF)	17.1	14.2	15	8.8
C_{ds} (fF)	13.02	14.1	10	14.0
g_{mo} (mS)	115	87.1	61	66.6
G_{ds} (mS)	12.0	11.2	12	8.7
R_i (Ω)	1.5	2.24	3.0	3.7
τ (ps)	0.23	0.17	0.2	0.32
f_T (GHz)	160	142	108	114
f_{max} (GHz)	187	164	130	150

Table I: Small signal equivalent circuit parameter and figures of merit for devices A, B & C; V_D=1.5V & V_G=0V.

Table I lists the small signal equivalent circuit parameters of the three devices. The experimental results are measured for device A. Table I reflects the close agreement between the measured parameters and the parameters extracted from the simulations. The transconductance is found to show a significant increase as the strain changes sign from compressive to tensile. This is due to the enhanced transport properties of the channel. The device figures of merit reflect the excellent performance potential of the devices under tensile strain. The maximum frequency of oscillation and the cut-off frequency given for the three types of device reflect the excellent performance potential of the devices with tensile strain.

It is to be noted that the bandgap decreases with increasing tensile strain, Eq.[3]. This dependence can have severe implications on the impact ionisation process. The reduced effective mass coupled with the reduced bandgap suggests the possibility of the onset of impact ionisation induced breakdown processes at much lower drain voltage conditions. However,

$$E_g^{tens}\left(In_{0.3}Ga_{0.7}As/In_{0.59}Al_{0.41}As\right)=0.85eV, \qquad (5)$$

while

$$E_g^{relax}\left(In_{0.53}Ga_{0.47}As/InP\right)=0.7eV \qquad (6)$$

[6], and the effective mass of the strained, low In content InGaAs channel is higher that of the $In_{0.53}Ga_{0.47}As$ channel on InP in the strain range of interest. Therefore it is expected that the transport enhancement of the low In content devices under tensile strain will be close to the InP based devices, but the breakdown behaviour will be better.

5. Conclusions

Control of the type and degree of strain offers an important degree of freedom in the design and realisation of high frequency HEMT devices. The characteristics of the devices obtained by proper engineering of strain would span a wide spectrum of low field mobility values as well as high field overshoot characteristics.

The transition from compressive strain to tensile strain results in devices with higher current drive capabilities, higher transconductance and an enhanced RF performance. Simulations have shown that the performance of HEMT devices may be improved with the use of InAlAs strain relief buffers. Simulations have shown that a 30% improvement in the cut-off frequency could be achieved using a tensile strained channel, while an 18% increase in current drive could thus be realised.

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References

1. P. Huang, T. Huang, H. Wang, E. Lin, Y. Shu, G. Dow, R. Lai, M. Biedenbender & J. Elliott: IEEE Trans. Microwave Theory & Tech **45** (1997) 2418.

2. M. Sexl, G. Bohm, D Xu, H Heiss, S. Kraus, G. Trankle & G. Weimann: J. of Crystal Growth 175 (1997) 915.

3. J. Thobel, L. Baudry, A. Cappy, P. Bourel and R. Fauquemberue: Appl. Phys Lett **46** (1990) 346.

4. J. Dickmann, K. Riepe, A. Geyer, B. Maile, A.Schurr, M. Berg & H. Daembkes: Japanese J. of Appl. Phys-1 **35** (1997) 10.

5. J. Chen, A. Li, Y. Ren & Y. Chang: J. of Crystal Growth **164** (1996) 460.

6. C.Kopf, H. Kosina & S. Selberherr: Solid State Electronics **41** (1997) 1139.

7. W.Hoke, P. Lyman, J. Mosca, H. Hendriks & A. Torabi: J. Appl Phys **81** (1997) 968.

8. S. Babiker, A. Asenov, J. R. Barker, S. P. Beaumont: Solid State Electronics **39** (1996) 629.

9. S. Babiker, A. Asenov, N. Cameron, S. P. Beaumont and J. R. Barker: IEEE Trans. Electron Devices **45** (1998) 1644.

10. S. Babiker, A. Asenov, N. Cameron, S. P. Beaumont: IEEE Trans. on Elect Devices **43** (1996) 2032.

11. T. Gonzàlez and D. Pardo: IEEE Trans. Electron Devices **42**, (1990) 605.