Three Dimensional Multi–grid Poisson Solver

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1. Introduction

Simulation–based analysis plays an important role in the design and development of semiconductor devices. A general trend in the electronics industry toward the development of devices with elaborate geometries and smaller dimensions has resulted in a need for more efficient and robust models to accurately determine electrical and physical characteristics. As device sizes decrease, the spatial distribution of the potential and/or current flow may become three-dimensional (3D) [1]. This causes one– and two–dimensional (2D) representations of the device to become invalid, resulting in a need for full 3D simulation tools.

In full 3D device simulations, the repeated solution of Poisson's equation dominates the execution time. Therefore, in order to reduce the computational burden in simulators, it is essential to implement fast and efficient Poisson solvers. The multi–grid method is one of the fastest techniques available to solve the Poisson equation [2]. In this paper a full 3D, inhomogeneous linear multi–grid Poisson solver is developed for device modeling applications in particle–based simulation tools, such as Monte Carlo and Cellular Automata. This algorithm represents the first such fully 3D multigrid solver for device simulation applications. As a test for the linear Poisson solver, a nonlinear version is developed using Newton's method and a 3D EEPROM (Electrically Erasable/Programmable Read Only Memory) device is modeled. The solution of the nonlinear Poisson equation will provide thermal equilibrium characteristics of the device.

The basic functionality of an EEPROM device, or floating gate transistor, is understood with a complete electrostatic analysis [3], making it an ideal application for this solver. The relationship between the threshold voltage and the floating gate charge in an EEPROM device is analyzed for various device geometries. Comparisons are then made with the solution of a 2D solver in order to determine 3D effects.

2. Newton Multi–grid Method

In general, Poisson's equation is a nonlinear equation, due to the dependence of the potential on the charge density. In thermal equilibrium, assuming nondegenerate conditions and homogeneous dielectric constant throughout the device, the nonlinear Poisson equation can be written as [4]

$$\nabla^2\psi(\mathbf{x}) = \frac{\alpha k_B T}{q n_i}\left(N_T - 2n_i \sinh(\frac{q\psi(\mathbf{x})}{k_B T})\right), \quad (1)$$

where $N_T = N_D - N_A$,is the total impurity concentration $\alpha = n_i q^2/\epsilon_s\epsilon_o k_B T$, q is the charge of an electron, n_i is the intrinsic carrier concentration, T is the temperature, and k_B is Boltzmann's constant. ψ, which is responsible for making the equation nonlinear, is defined as

$$\psi(\mathbf{x}) = -(E_i(\mathbf{x}) - E_f)/q. \quad (2)$$

the difference between the Fermi energy, E_f, and the intrinsic Fermi energy, $E_i(\mathbf{x})$, divided by q. Discretizing the Poisson equation on a grid, Ω_n and then applying Newton's method results in the set of linear equations

$$\mathbf{J}^j\mathbf{d}^j = \frac{q}{\epsilon_s\epsilon_0}\left(\mathbf{N}_T - 2n_i \sinh(\frac{q\psi^j(\mathbf{x})}{k_B T})\right) - \mathbf{L}\psi^j(\mathbf{x}), \quad (3)$$

L is the discretized Laplacian operator and the Jacobian, $\mathbf{J}^j$ is

$$\mathbf{J}^j = \mathbf{L} + 2\alpha\cosh(\frac{q\psi^j(\mathbf{x})}{k_B T}). \quad (4)$$

This set of linear equations is then solved using an iterative multi–grid algorithm, and the next approximation to the solution is found with the equation

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$$\psi(\mathbf{x})^{j+1} = \psi(\mathbf{x})^{j} + \mathbf{d}^{j}. \quad (5)$$

3. EEPROM

In recent years, the market for nonvolatile memory devices has grown rapidly. This trend should continue, especially for flash memory cells [5]. Flash memories are devices in which a single cell can be programmed and a large block of these cells can be electrically erased simultaneously. EEPROM devices are currently too large, and therefore too expensive, to be manufactured for anything except very specific applications. New architectural designs are being explored in order to design EEPROM devices for a wider range of applications. The floating gate transistor as shown in Fig. 1 meets the requirements of a very compact layout, with suitable performance and future scalability [5].

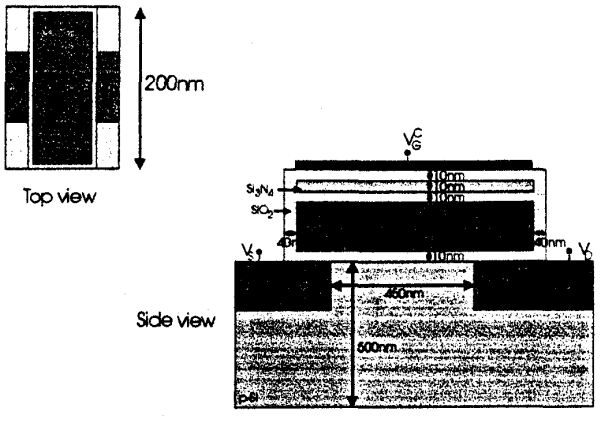

Figure 1: Schematic layout of the simulated floating gate EEPROM device; the p-Si is doped $N_A = 1 \times 10^{17} cm^{-3}$ and the n-Si is doped $N_D = 1 \times 10^{18} cm^{-3}$.

A memory cell needs to commute from one state to another, and information needs to be stored independently of external conditions. The EEPROM illustrated in Fig. 1 works by storing charge in the floating gate. The role of this stored charge is to shift the drain current versus gate-to-source voltage curve. The threshold voltage is higher when there is charge stored in the floating gate. Therefore, the two states of the transistor correspond to the gate containing and not containing charge.

The switching time between states is proportional to the change in threshold voltage. To understand the dependence of the threshold voltage on the gate charge and the device geometry the EEPROM may be treated as an electrostatic problem. This analysis is valid because it is only important to determine the charge on the gate at the onset of inversion, which means there is no current in the device, hence an ideal device to test the nonlinear Poisson solver.

The EEPROM is simulated in 2D and 3D to demonstrate the influence of the device geometry on the threshold voltage. The 2D simulation illustrates the change in threshold voltage as a function of the channel length between the source and drain, while the 3D simulation is necessary to model the threshold voltage shift as a function of the width of the source and drain.

The floating gate of the EEPROM is modeled as a metal. In a real EEPROM device the floating gate is made of highly doped polysilicon, but the Poisson solver is not able to determine how the charge is distributed in the floating gate. The charges in the floating gate determine a threshold voltage value, so by treating the gate as a metal the threshold voltage can be set and the corresponding floating gate charge can be calculated.

2D Model

The electrical behavior of the 2D EEPROM device shown in Fig. 1 can be understood by analyzing the schematic layout in Fig. 2. The total charge stored

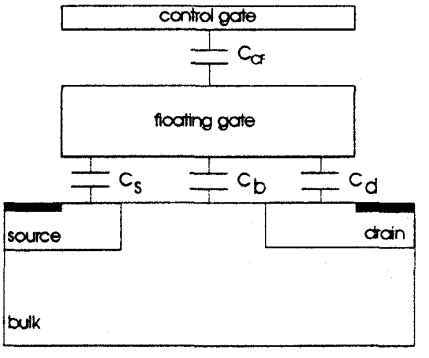

Figure 2: Schematic of 2D EEPROM, showing various capacitances [3].

in the floating gate can be written as [3],

$$\begin{aligned} Q_{FG} &= C_{CF}(\phi_G^f - \phi_G^c) + C_S(\phi_G^f) \\ &+ C_B(\phi_G^f - \phi_B) + C_D(\phi_G^f - \phi_D), \end{aligned} \quad (6)$$

where C_{CF}, C_S, C_B, and C_D are capacitances between the control gate and floating gate, floating gate and source, floating gate and bulk, and floating gate and drain, respectively and are shown in Fig. 2. ϕ_G^f, ϕ_G^c, ϕ_B, and ϕ_D are the potentials on the floating gate, control gate, bulk and drain respectively referenced to the source. Because this is an electrostatic simulation, the device is biased so that it is at the onset of inversion, and the equation can be written as,

$$V_t = -\frac{Q_{FG}}{C_{CF}} + V_{t0}, \quad (7)$$

where V_{t0} is the threshold voltage when $Q_{FG} = 0$.

In the simulation, the device is discretized using an inhomogeneous grid spacing. The channel length between the source and drain is then reduced from 450nm

to 150nm in such a way that the difference between the drain n-doped region and the source n-doped region is always 150nm. At each channel length the total charge on the floating gate is calculated for a series of the threshold voltages. The results are presented in Fig. 3.

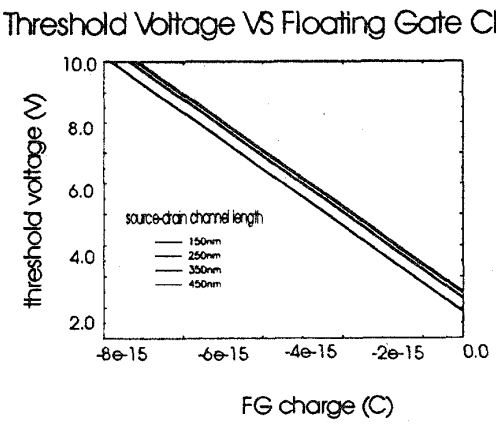

Figure 3: Simulated threshold voltage versus floating gate charge for the 2D EEPROM for various source-to-drain channel lengths.

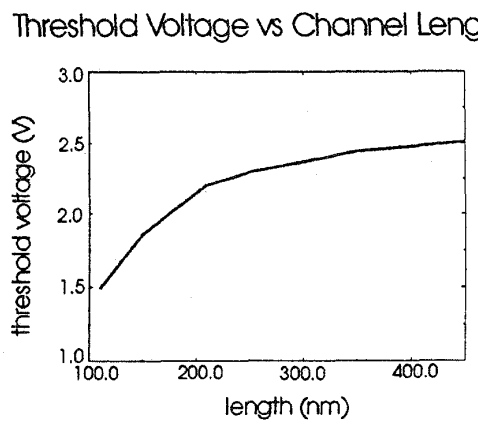

Figure 4: Plot of the threshold voltage versus source-to-drain channel lengths for 2D EEPROM, for zero floating gate charge.

As the channel length between the source and drain is changed in the simulation, the capacitances between the floating gate and the control gate remain constant. This can be seen in Fig. 3. On the other hand, the capacitances due to the source, bulk, and drain do change, which affects V_{t0}. A plot of the change in V_{t0} with respect to channel length is given in Fig. 4. As shown in the figure, the threshold voltage saturates at long channel lengths.

3D Model

In the full 3D simulated transistor, shown in Fig. 1, the width of the source and drain are modulated with respect to the floating gate. The coupled capacitance between the source and floating gate, and that between the drain and floating gate then changes. Initially, the source and drain widths are set equal to the width of the floating gate, then they are subsequently reduced. As these widths are reduced, the region under the floating gate is replaced with SiO_2. At each width, the floating gate charge is calculated along with the corresponding threshold voltage. The resulting plots, presented in Figs. 5 and 6, show a change in the zero charge threshold voltage with respect to the source/drain width.

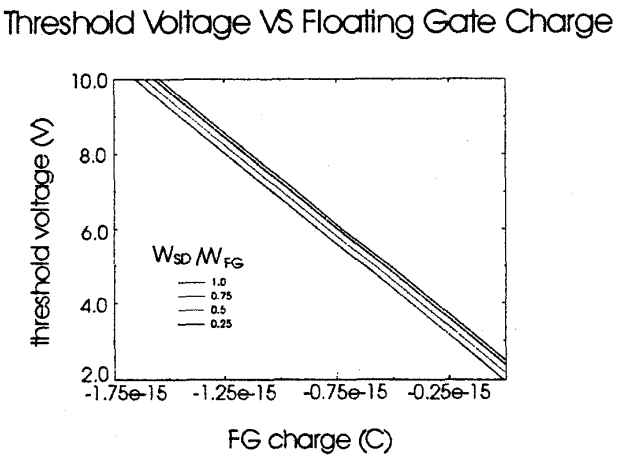

Figure 5: 3D EEPROM threshold voltage versus floating gate charge for various source-drain widths. W_{SD} is the source-drain width and W_{FG} is the floating gate width.

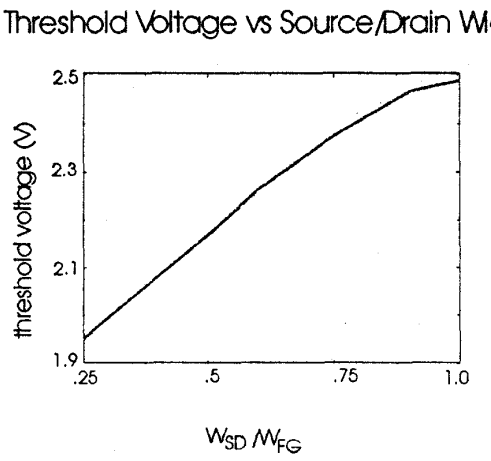

Figure 6: 3D EEPROM threshold voltage vs source-drain widths, for zero floating gate charge. W_{SD} is the source-drain width and W_{FG} is the floating gate width.

4. Conclusion

The Newton Multigrid Method was shown to be an effective method for solving the nonlinear Poisson's equa-

tion for semiconductor devices under thermal equilibrium conditions. This technique can also be used to solve problems involving reverse bias junctions. Assuming an insignificant concentration of minority carriers, such that no leakage current is present, and fixing the quasi-Fermi potential as a constant for majority carriers, the nonlinear Poisson's equation can be used to simulate such situations.

The program was successfully applied to simulate 2D and 3D EEPROM devices. The widths of the source and drain regions were modulated to determine the influence of 2D and 3D effects on the capacitance. In both the 2D and 3D cases, reducing the channel size resulted in a decrease in the zero charge floating gate threshold voltage, while the capacitance between the control gate and floating gate remained constant. When the channel length is shorter, there is more overlap of the source and drain depletion region. Therefore less voltage is needed to reach threshold, which in turn increases the speed of the device. The change in threshold voltage is less pronounced in the 3D simulation. When the channel width is modulated, the effect of decreasing the active region results in a decrease in the amount of voltage needed to reach threshold. For design optimization, it is necessary to create a transistor which has the smallest change in threshold voltage, with a resulting shorter switching time and a therefore faster response.

References

[1] R. Kircher and W. Bergner, *Three-dimensional Simulation of semiconductor devices*, vol. 1. Birkhäuser Verlag, 1991.

[2] R. P. Fedorenko, "A relaxation method for solving elliptical difference equations," *USSR Comp. Math. math. Phys.*, vol. 1, no. 5, pp. 1092–1096, 1961.

[3] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash memory cells - an overview," *Proceedings of the IEEE*, vol. 85, pp. 1248–1271, August 1997.

[4] R. F. Pierret and G. W. Neudeck, *Modular series on solid state devices; Advanced semiconductor fundamentals*, vol. 6. Addison-Wesley Publishing Company, 1989.

[5] S. Keeney, R. Bez, D. Cantarelli, F. Piccinini, A. Mathewson, L.Ravazzi, and C.Lombardi, "Complete transient simulation of flash EEPROM devices," *IEEE Transactions on Electron Devices*, vol. 39, pp. 2250–2757, December 1992.