Fundamental Operation and Design Considerations for Metal-Oxide Tunnel Transistors

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The ideal tunneling operation, materials, and geometrical design considerations for novel field-effect transistors which do not employ dopants of any kind are given. Non ideal effects on the performance, such as the effects of scattering and excess-space charge, are also simulated.

I. Introduction

Further progress in integrated-circuit (IC) technology is limited by short-channel effects and by the physical size of the area taken up by the source and drain contacts, doping wells, and isolations. The random location of dopants is also expected to create fluctuations in the threshold voltage of individual transistors. An approach to the continued down scaling of silicon IC is based on quantum tunneling in the silicide/silicon system [1-2]. Another approach is to replace this with non-semiconductors, e.g., metal-oxide tunnel transistor (MOTT) [3-5].

We focus on the simulation of the tunneling current which is the basis of operation of MOTT. The results are applicable to silicide/silicon system. The dependence of the gate control on the aspect ratio of the thickness-to-the-width of the tunneling oxide is investigated using a 2-D fast Poisson solver [5] and/or analytical expression for the potential of a uniform channel-width device. MOTT has the capability to operate as a transistors with useful gain for aspect ratio considerably less than one. Numerically solving the Schrodinger equation allows us to investigate the quantum interference effects. There are three modes of current transport as a function of drain bias.

For a given aspect ratio, the output impedance improves with increase in tunnel-oxide width, accompanied by slight decrease of gate transconductance. The net result is a significant improvement in the transistor gain. The gate transconductance improves with decrease in gate-insulator thickness, while approximately maintaining the output impedance. The net result is also a significant improvement in the transistor gain. Thus, for a given aspect ratio further increase in the transistor gain can be carried out by increasing the tunnel oxide width and/or decreasing the gate insulator thickness. Uniform-oxide channel design is generally superior to tapered-oxide channel designs.

The effects of scattering and excess-space charge in the channel are to suppress the current values and to greatly straighten the ideal sharp 'knee' point of the current-voltage (I-V) tunneling characteristics. Our results accounting for scattering and excess space charge qualitatively agrees with our experiments on Nb / NbO_x / Nb tunnel transistors.

2. Gate Control in MOTT

A cross-sectional view of a MOTT and the energy diagram across the source/tunnel-oxide/drain region of MOTT under bias are schematically shown in Fig. 1.

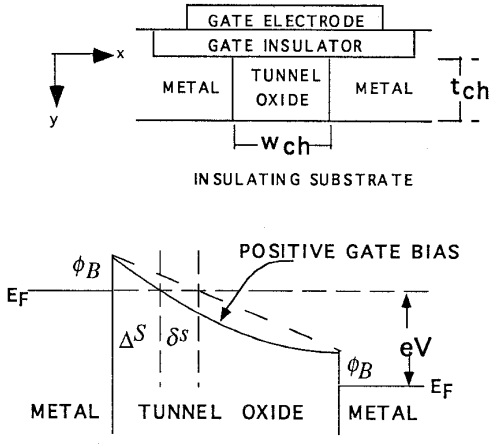

Figure 1: MOTT cross section and energy band diagram

The essential action of a gate-bias is to modulate the tunneling width, ΔS, thereby also modulating the tunneling current. For a useful transistor action, the following

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conditions must be met, namely, (a) exponential control of the source-drain current by the gate bias to obtain high transconductance, and (2) sufficient screening of the drain-bias by the gate-induced polarization charge so that the tunneling potential width at the source is nearly independent of the drain bias, resulting in high output impedance.

For a MOTT with uniform channel width, the 2-D potential profile in the channel, with the source at ground potential, may be given an analytical expression as

$$\varphi_{ch}(x,y) = -\phi_B + V_g + \left(\frac{V_D - V_g + V_g \cosh(w_{ch}/\lambda)}{\sinh(w_{ch}/\lambda)} \right) \sinh(x/\lambda) - V_g \cosh(x/\lambda), \quad (1)$$

ϕ_B is the barrier height, V_g and V_D are the gate and drain biases respectively, w_{ch} is the channel width, and λ is given by

$$\frac{\lambda^2}{w_{ch}^2} = \left\{ \frac{e_{tox}}{e_g} \left(\frac{t_g}{w_{ch}} \right) \left(\frac{t_{ch}}{w_{ch}} \right) + \frac{y}{w_{ch}} \left(\frac{t_{ch}}{w_{ch}} \right) - \frac{y^2}{2w_{ch}^2} \right\}, \quad (2)$$

where e_{tox}/e_g is the ratio of dielectric constants of the channel to the gate insulator, t_{ch} and t_g are the channel and gate insulator thicknesses, respectively.

The y-dependent parameter given by w_{ch}^2/λ^2 measures the charge density due to the polarization in the x-direction induced by the gate in the channel. The two conditions given above for transistor action are met if this parameter is maximized (optimized) in the device design. The aspect ratio $R = t_{ch}/w_{ch}$ must therefore be made considerably less than one [5]. The optimization of this aspect ratio is the major design consideration upon which further fine tuning of the device performance has to be carried out.

3. Operating principle of MOTT

For positive gate bias, there are basically three carrier transport modes across the tunnel oxide with increasing drain bias voltage, namely, (a) the shifting double-barrier (SDB) mode, (b) onset of the single-barrier tunneling (OSBT) mode, and (c) the single-barrier tunneling (SBT) carrier transport mode.

The SDB mode is characterized by a rapid increase in source-drain current which varies linearly with the drain bias. The SDB mode is also characterized by the resonant, i.e., oscillating, behavior of the current as a function of drain bias in the presence of coherence effects [6]. For realistic MOTT at room temperature, quantum coherence will be washed out by scattering in the oxide.

Further increase in drain bias will lead to the OSBT mode of operation whereby single-barrier mode of tunneling begins to be the dominant carrier transport mechanism across the oxide width. This is characterized by a decreasing rate of increase of the source-drain current with increase in the drain bias, producing a 'knee' region in the I-V plot.

At higher drain bias, the transistor goes into the SBT mode whereby the current is entirely controlled by a single-barrier tunneling mechanism. Depending on the aspect ratio of the MOTT device [5], this mode exhibits a 'saturation' current behavior in the range of interest in low-voltage ultra large-scale integrated circuits.

4. MOTT gain versus device parameters

From our simulation results, we estimate the transfer-characteristic (TC) voltage gain, $G(V_d, V_g)$, by calculating this at any point (V_d, V_g) simulating the (V_{out}, V_{in}) in the TC of coupled logic gates [7] , as

$$G(V_d, V_g) \approx \frac{g_m}{g_D}, \quad (3)$$

where g_m is the transconductance and $1/g_D$ is the output impedance.

Dependence on aspect ratio, *R*

Figure 2a shows the calculated TC voltage gain for a Nb / NbO_x / Nb MOTT, with $R = 7/30$. Figure 2b shows the corresponding TC voltage gain for $R = 1/6$.

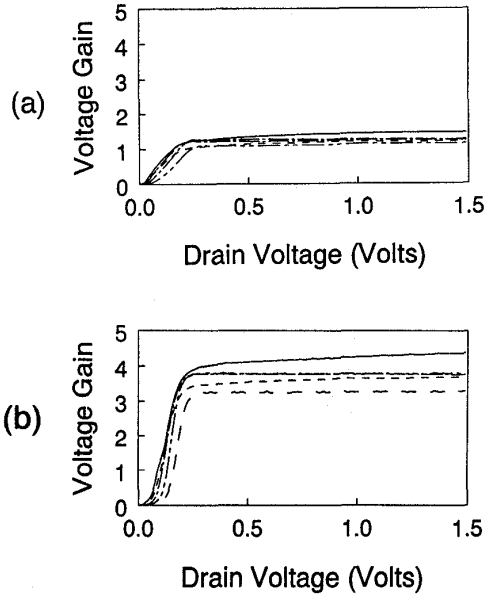

Figure 2: TC gain as function of V_D for V_g=0.0, 0.5, 1.0, 1.5, and 2.0 eV: (a) for R=7/30 and (b) for R=1/6.

These two figures show about three times improvement in the TC voltage gain upon decreasing the aspect ratio from $7/30$ to $1/6$.

Dependence on tunnel-oxide width, w_{ch}

Holding the gate insulator thickness and the aspect ratio constant, the tunnel oxide width of MOTT of Fig. 2a is increased from 30 nm to 60 nm with corresponding increase in channel thickness to 14 nm. The calculated TC voltage gain yields two times improvement by doubling the tunnel-oxide width when compared to Fig. 2a.

Dependence on gate insulator thickness, t_g

Holding the aspect ratio and tunnel-oxide width of the MOTT of Fig. 2a constant, the gate insulator thickness is increased from 10 nm to 15 nm. The calculated gain for the 15 nm gate-insulator thick MOTT is lower by about 50% than those of Fig. 2a for a thinner gate insulator thickness of 10 nm.

Dependence on channel shape

Depending on the duration of the oxidation process, thickness of the metal layer, and on which side of the metal layer the consequent processing of the gate insulator and gate metallization is formed, one may either obtain a tunnel oxide which tapers in, having a smaller width near the gate, or a tunnel oxide which tapers out, having a larger width near the gate. The typical potential-surface distributions, calculated using a fast Poisson solver, for tapered-in and tapered-out tunnel oxides are depicted in Figs. 3 and 4, respectively, shown for $V_g = 0.5\,V$ and $V_d = 0.5\,V$.

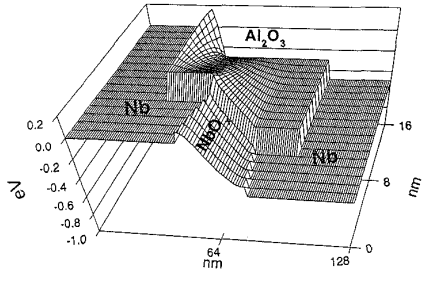

Figure 3: Surface plot of electron potential inside the tapered-in channel MOTT

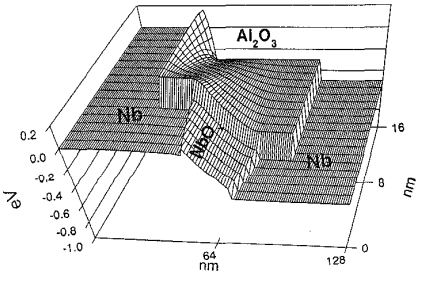

Figure 4: Surface plot of the electron potential inside the tapered-out channel MOTT

Whereas the tunneling-potential profiles for the uniform-channel devices are approximately triangular at the source region throughout the oxide thickness, these are far from being triangular at or near the source region in most of the oxide thickness for the tapered-channel devices. This difference leads to lower current values and degradation of performance compared to the corresponding uniform channel MOTT. For tapered devices output impedance and transconductance do not go together in contrast with that of uniform channel devices.

Although the tapered-out channel tends to have higher output impedance than the tapered-in channel, the tapered-in channel has higher transconductance than the tapered-out channel design. These compensating values between the impedances and transconductances in both tapered channel designs lead to equal estimated values of their TC voltage gain, which are inferior to that of the corresponding uniform channel design.

The calculated gain of tapered-in (30 nm width at oxide/substrate interface and 16 nm width at the oxide/gate-insulator interface) and tapered-out (16 nm width at oxide/substrate interface and 30 nm width at the oxide/gate-insulator interface) devices, respectively, show more than 60% lower value compared to the corresponding uniform-channel MOTT.

Dependence on barrier height, ϕ_B

Figures 5 and 6 show the calculated gain of the simulated MOTT with $R = 1/6$ when ϕ_B is changed from 0.1 eV to 0.2 eV and 0.3 eV, respectively.

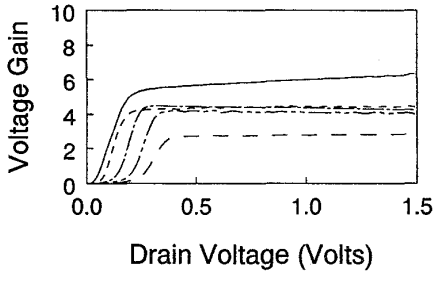

Figure 5: TC gain for ϕ_B=0.2 eV and $R = 1/6$

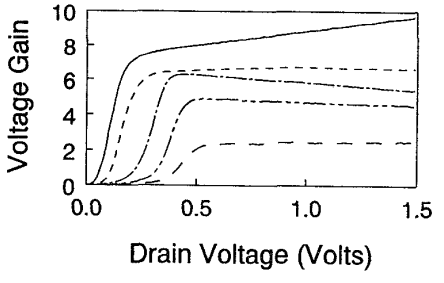

Figure 6: TC gain for ϕ_B=0.3 eV and $R = 1/6$

The calculated gains have average values which are apparently independent of the barrier heights (from Figs. 2b, 5 and 6), however, the spread of the gain for different gate

biases increases with increase in ϕ_B. The gain becomes more indeterminate as the barrier height increases, and in the limit of large-enough barrier height resulting in zero current, the gain becomes completely indeterminate.

Dependence on temperature

The calculated gain of the simulated MOTT with aspect ratio of $1/6$ when the temperature is lowered to 77K is also calculated. The resulting average value of the voltage gain does not seem to be affected, but the spreading is reminiscent of the effect of increasing the barrier height.

5. Scattering and excess-space charge

We investigated the effects of scattering and excess space charge in the channel by solving the drift-diffusion and Poisson equations self-consistently within the channel. The current density given by

$$J = \frac{emk_B T}{2\pi^2 \hbar^3} \int_0^\infty \left[T^+(E) N^+(E) - T^-(E) N^-(E, V_D) \right] dE \quad (4)$$

is adjusted according to the self-consistent potential in the channel. $T^+(E)$ and $T^-(E)$ are the transmission coefficients from the source and drain, respectively, and obtained by solving the Schrodinger equation for a given potential. This is accomplished by rewriting the Schrodinger equation in terms of the logarithmic derivatives of the wavefunction, $Z(x,E)$, solved through a recursion relation yielding $Z(x_{i+1},E)$ in terms of $Z(x_i,E)$ for the piecewise continuous segments of the potential profile. The transmission coefficients are obtained from the $Z's$ [8-10]. $N^+(E)$ and $N^-(E,V_D)$ are electron supply functions at the source and drain, respectively.

Once the current is determined, the excess-space charge is calculated from the drift-diffusion equation by another recursion relation between the discretized potential mesh points. We found a stable recursion by starting from the drain region with known electron density at the contact. The potential is recalculated with the new space charge in the channel and the whole procedure repeated until convergence is obtained. In our preliminary calculations, we used $\mu = 10.0\ cm^2 / Volt - \text{sec}$ and $v_s = 10^7\ cm / \text{sec}$.

Figure 7 shows the effects of scattering and excess space charge on the I-V characteristics of the MOTT with R=1/6.

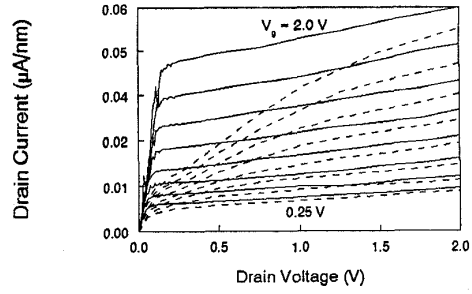

Figure 7: I-V characteristics of simulated MOTT with $R = 1/6$, V_g=0.25, 0.5, 0.75, 1.0, 1.25, 1.5, 1.75, and 2.0 eV. Solid curve (without) and dotted curve (with) scattering and space charge effects.

Scattering and excess-space charge in the channel yield lower current values and greatly soften the ideal sharp 'knee' point of the I-V tunneling characteristics, particularly at large gate bias. These results qualitatively agree with our experiments on $Nb / NbO_x / Nb$ tunnel transistors. We are currently exploring other metal-oxide and Schottky-barrier systems, as well as the idea of merging the conventional field-effect gate control and quantum tunneling in novel device designs.

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