Parallel Processor System Specific for Monte Carlo Analysis Based on Ring Bus Architecture

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We have developed a new parallel processor system specific for the MC analysis, to dramatically reduce the calculation time. Our parallel processor system is based on ring bus architecture. The RISC micro processor chip, which contains a ring bus interface unit (RBIU), a floating point arithmetic unit (FAU) and so on , was also developed for our system. Speed up ratio compared with a single processor reached to 13.5 at 23 PEs.

1. Introduction

The device simulation based on the Monte Carlo(MC) analysis is very useful for analyzing the phenomena such as the hot carrier effect and the non-stationery effect in an ultra small MOS transistor with the gate length of less than 0.1 μ m. However, the device simulation based on MC analysis consumes a huge computational time because it is necessary to increase the number of traced particles and the tracing time steps in order to improve the accuracy in the simulation. Then we have developed a new parallel processor system specific for the MC analysis, to dramatically reduce the calculation time.

2. Ring Bus Architecture

The parallel calculation of carriers motion can be achieved effectively in loosely coupled multi-processor systems since the calculation corresponding to each of arithmetic nodes can be performed almost exclusively without costly inter-processor communications. The uni-directional ring-bus architecture, which is one of loosely coupled multi-processor architectures as shown in Fig.1, has the advantage over the other architectures. It can be constructed with much more processing nodes as compared

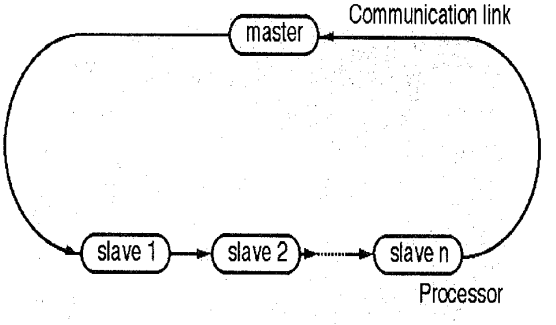

Fig. 1 Ring bus connection.

with tightly coupled multi-processor networks such as shared bus or shared memory architecture because loosely coupled networks do not suffer from growth of bus contention or electrical load by increasing nodes. It has only two communication ports and high-bandwidth can be achieved without expensive implementation technologies.

The calculation time for motion of particles is reduced rapidly with increasing the number of processor nodes. And then the calculation time of potential equation can not be ignored any more. Therefor, potential equation should be also solved in parallel by using parallel computer system. Potential calculation requires more frequent communication

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between processor nodes in general. Fortunately, SOR method with red-black ordering for solving potential equation is also easily implemented on the ring bus architecture.

The MC simulation flow of a paralleled program is shown in Fig.2. To execute this simulation flow, we employ the ring bus architecture with one master processor and many slave processors. The master processor is used to control the whole flow in the parallel simulation, and to distribute the data and to collect them. The slave processors are used to solve the Poisson's equation and Newton's equation in parallel being supervised by the master processor. The bus with a high data transfer speed is essential to achieve a high performance parallel processor system. MC simulation requires the two types of the communication between processors. One is the communication between one processor and the other processors, which is occurred when initializing the processor, transferring the charge data and potential data and so on. The other is the communication between the adjacent processors, which is occurred during potential calculation.

In order to satisfy this communication requirement, our designed ring bus has three operating modes as show in Fig.3. Mode 0(Basic transfer mode) and Mode 1(Token passing mode) are designed for communication between one processor and the other. Mode 3(Ring transfer mode) is designed for communication between the adjacent processors.

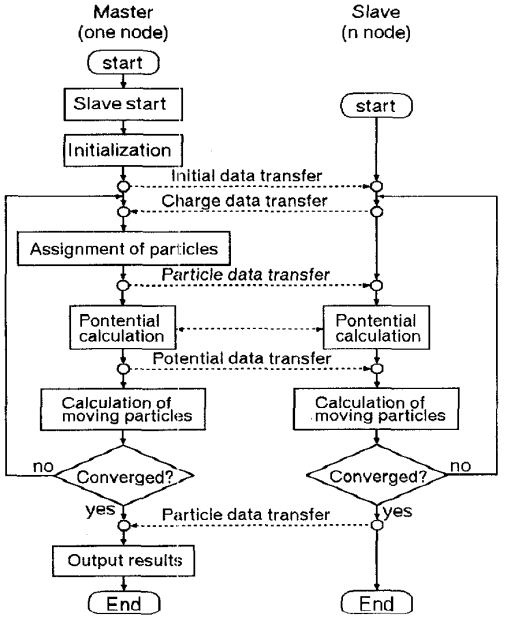


Fig. 2 Flowchart of Monte Carlo device simulation for parallel processor system.

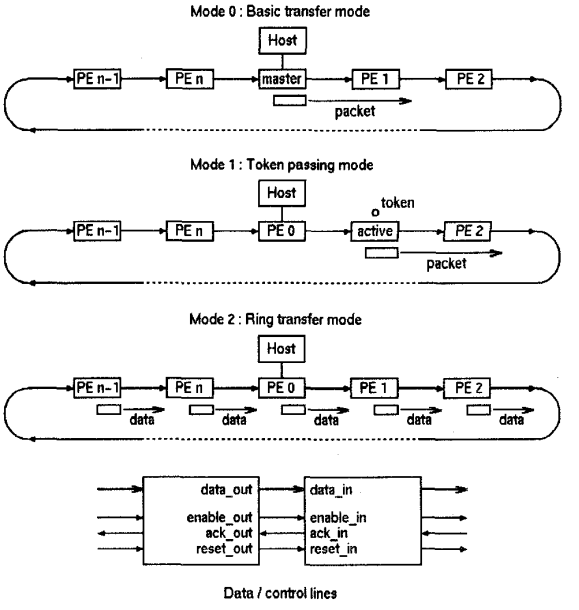


Fig. 3 Ring bus operating modes.

Mode 0 is the high speed synchronous data transfer mode in which the data transfer operation between the master processor and the slave processors is executed based on the master-slave operation method. Mode 1 is also the high speed synchronous data transfer mode in which, however, all of the processors are even in access and the scheduling is carried out using the token passing method. In the mode 0 and model, the data form a packet and this packet is transferred with a very high speed through the ring-bus. In addition, a high speed DMA data transfer method is employed in these two modes.

Mode 2 is used to transfer the data to the adjacent processor. The data do not form the packet in this mode. The hand-shake type data transfer method is employed. Therefore, the data transfer speed in the mode 2 is necessarily slower than those in previous modes because the occupancy of the buffer in the processor to receive the data should be checked before the data transfer. However, it is possible in the mode 2 to transfer the data among many pairs of adjacent processors in parallel. Therefore, the overall data transfer speed becomes considerably high when it is required that many processors send the data simultaneously to their adjacent processors. This mode can be used to simultaneously transfer the data for the peripheral meshes in a block to the adjacent processors in solving the Poisson's equation in parallel.

3. RISC Processor Chip Design and Fabrication

In order to achieve the ring bus operation described

above, we developed a RISC microprocessor chip as shown in Fig.4. The chip contains a ring bus interface unit (RBIU), an integer arithmetic unit (IAU), a floating point arithmetic unit (FAU), an instruction cache unit (ICU) , and a memory interface unit (MIU).

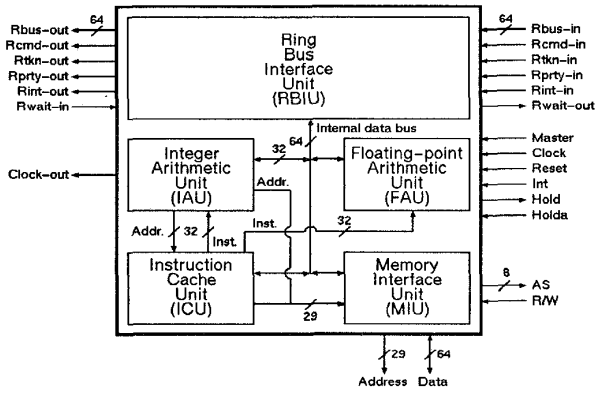


Fig. 4 Block diagram of the chip.

The IAU performs 32bit integer arithmetic computations and steers overall functions on the chip. The FAU can operate IEEE-754 double precision floating-point arithmetic addition/subtraction in parallel with multiplication /division. Each of the IAU and the FAU can decode and execute own instruction field of a VLIW (Very Long Instruction Word) synchronously.

The chip integrates 580k transistors in 14.27x13.60mm^2 area using standard CMOS 0.65 μ m, 2-metal technology. The chip micrograph is shown in Fig.5.

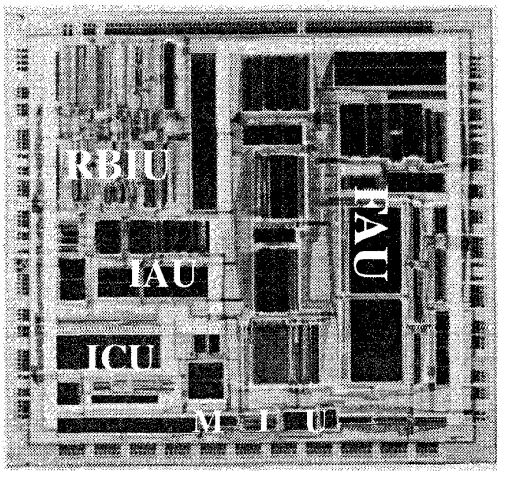


Fig. 5 The chip micrograph.

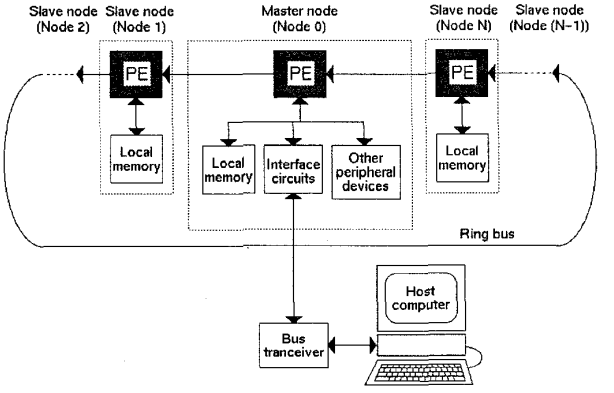


Fig. 6 System block diagram.

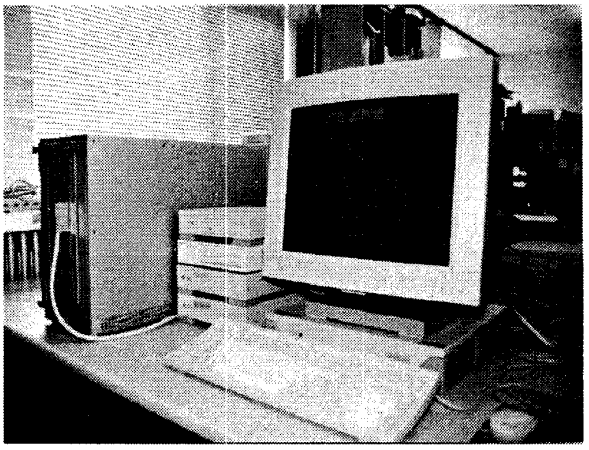
4. System Configuration and Specification

The whole configuration of our parallel processor system is shown in Fig.6. This figure shows that one master node and many slave nodes are connected in the ring-bus. Slave processor nodes consist of RISC processor chip, and a local memory of 1MB. The master node has the interface circuits to communicate with the host computer in addition to the local memory of 8MB. To execute the simulation the program is transferred from the host computer through the interface circuits to the master node at first. Then, the master node broadcast the program to all of the slave nodes. After that, the whole programs run and the processor nodes execute the potential calculation and the calculation to solve the kinetic equation. In this case, the master node has the roles to synchronize the whole programs and to inform the states of calculations to the host computer. After the calculations are completed, the master node collects the calculation results from all of the slave nodes and transfers them to the host computer.

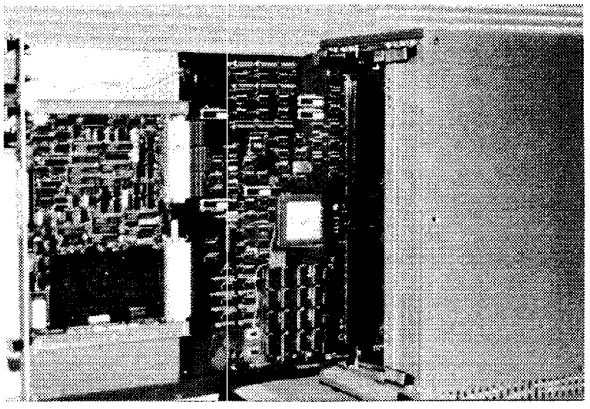
Fig.7 shows photographs of parallel computer system specific for Monte Carlo simulation. Fig. 7 (a) shows the simulation engine (the left side) and Sun SPARC station 20 (the right side) as a host computer. Fig.7 (b) shows a master board that contains a master node, and Fig. 7(c) shows a slave board that contains eight of slave nodes. The physical size of simulation engine is 23cm×66cm×45cm. This is a very compact size as compared with other general purpose parallel computer system.

5. Performance Evaluation and Analysis

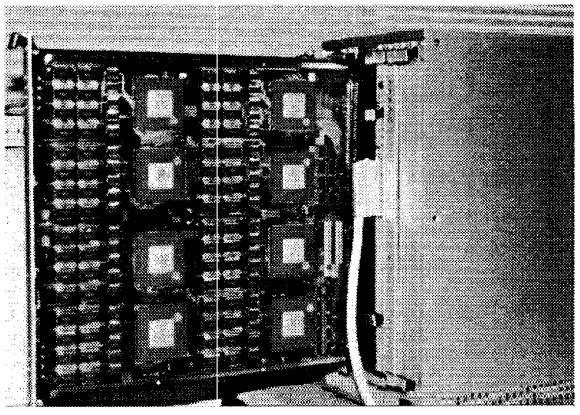
We confirmed the MC simulation worked well on our parallel computer system. Then, computation time has been measured using the simulation engine with 9, 17 and 23 nodes. Figure 8 plots the relation between the number of PE and speed up ratio compared with a single processor.



(a) Parallel processing system connected with host computer.



(b) Master board.



(c) Slave board contained eight of slave nodes.

Fig.7 Photographs of parallel computer system specific for Monte Carlo simulation.

Both the speed up ratio corresponding to calculation for motion of particles and that corresponding to calculation of potential are plotted in addition to the total speed up. It reached to 13.5 at 23 PEs. The speed up curve of calculation for motion of particles is similar to ideal one, while that of potential calculation drops gradually. And the total speed up ratio is ristricted by the speed up of potential calculation. We identified two reasons why the speed up in the potential calculation tends to saturate in our system. One is that the transport overhead on ring transfer mode increases considerably as the data size becomes larger. The other reason is that our system has no function dedicated to inter-processor synchronisation in ring transfer mode.

In order to improve these problems, we have been designing the next system which would improve the communication performance by an additional ring bus operating mode that can synchronously transport a large amount of data without significant overhead.

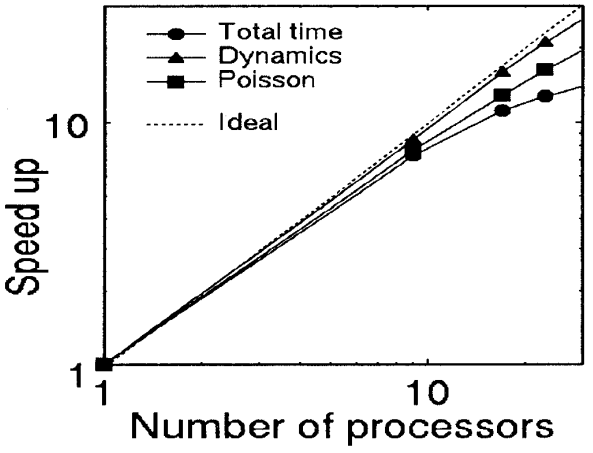


Fig. 8 Speed-up of Monte Carlo simulation.

3. Summary

We have developed a new parallel processor system specific for the MC analysis, to dramatically reduce the calculation time. Our system is based on ring bus architecture. Speed up ratio compared with a single processor reached to 13.5 at 23 PEs. We have been designing the next system which would improve the communication performance by a new ring bus operation mode.

References

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