Hybrid circuit simulator for combined single electronic and conventional circuit elements

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Single electron tunneling (SET) devices have been studied extensively due to their promise for realizing extremely high gate density with ultra-small power dissipation. However, issues are the inherent low voltage gain and the low driving capability, which are critical drawbacks for implementing SET logic gates. A voltage gain defined as capacitance ratio of a gate to a tunnel junction of SET transistor must be much greater than unity to drive next stage devices, while it is very difficult to fabricate a SET transistor with large gate capacitance and small junction capacitance. A few electrons employed in SET devices cause output voltage fluctuation. One of the solutions to overcome these problems is to develop a hybrid circuit consisting of SET devices and MOSFETs. Such a hybrid circuit has been experimentally demonstrated[1]. We report a hybrid circuit simulator for the analysis of such hybrid circuits.

The hybrid circuit simulator is composed of a conventional circuit simulator, SPICE, and a SET circuit simulator. In the simulator, a SET device consisting of tunnel junctions and capacitors is treated as a black box element like a MOSFET model represented with resistors, capacitors, current sources and diodes. The black box element is one of the elements included in SPICE such as resistors, capacitors, inductors, diodes, bipolar transistors, MOSFETs and other elements. A main routine of SPICE provides node voltages and time step to each element, and then the element calculates node currents and conductances which are fed back to the main routine (Fig. 1). The main routine solves a circuit equation $\mathbf{YV} = \mathbf{I}$ satisfying Kirchhoff's current and voltage laws (KCL and KVL) by using a Newton-Raphson iterative algorithm, where $\mathbf{Y}$ is a node admittance matrix in which each element is defined as current derivative, $\mathbf{V}$ is a node potential vector, and $\mathbf{I}$ is an equivalent node current source vector.

There are two alternative ways to analyze the behavior of SET circuits: a master equation (ME) method based on probabilities for several charge configurations and a Monte Carlo (MC) method to simulate real motion of electrons in a system. In the ME method, current is treated as a *continuous* value so that its derivative can be analytically calculated because the current value fed back to the SPICE main routine is calculated as an average value weighted by probabilities. Thus it is easy to implement a black box SET element in the ME method. In the MC method, however, the current is obtained as a time-averaged value of the tunneling electrons through a node, hence the current changes *discretely*. For the MC method, either large SPICE time step or current from/to the black box element is used for stable numerical calculation in the SPICE main routine.

The current returned to the SPICE main routine consists of three parts. The first one is the current tunneling through tunnel junctions. The second is the polarization current induced by the change of the number of electrons in internal nodes of a black box element. In the ME method both currents above are analytically calculated by using probabilities based on the solution of the master equation, while in the MC method they are calculated as average values during a given time step. The last one is the polarization current induced by the direct influence of voltage change in external nodes, which is calculated from a capacitance matrix of circuit element models.

Amakawa et al[2] reported a hybrid circuit simulator aiming at fast calculation of electrical characteristics of large scale circuits composed of SET transistors and conventional elements. In the simulator, a simple SET transistor model calculated from a steady-state ME method is used. Thus, no SET devices with hysteresis such as a turnstile and SET memory can be simulated.

Figure 2(b) shows calculated characteristics of an asymmetric turnstile[3] of Fig. 2(a) , which are calculated with a stand-alone SET circuit simulator based on a ME method (solid lines), a hybrid circuit simulator on a ME method (solid circles), and a hybrid circuit simulator on a MC method (open squares). The results are in good agreement with each other. The hybrid circuit simulator on the ME method provides correct results only for relatively small time step (in this case, $\Delta t = 10^{-9}$sec) because numerical integration error of current from/to the turnstile increases with the value of the time step. The MC method using large time step ($\Delta t = 5 \times 10^{-5}$) can save CPU time significantly.

Figure 3(a) shows a SET counter circuit[3] consisting of an asymmetric turnstile and complementary MOSFET inverters. Figure 3(b) shows the

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output waveforms of the turnstile and the second inverter under the saw-tooth input gate voltage calculated by a hybrid simulator based on a ME method. The output of the second inverter flips after 39 gate clock cycles at which the output voltage of the turnstile exceeds the inverter threshold.

SET devices can be classified into two categories according to current flow mechanism. One is the devices called dynamic-SET devices, such as a SET transistors, through which charges move *dynamically.* Another is the devices called static-SET devices, such as a turnstile, through which charges transfer *statistically* under control. We realized the following facts through various circuit simulations. Although dynamic-SET devices connected to large load capacitors can be simulated with a hybrid circuit simulator based on a ME method, for the other hybrid circuits including static-SETs and dynamic-SETs with small load capacitors, a hybrid simulator with a MC method is the best choice in terms of CPU time used.

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References

[1] A. Ohata, A. Toriumi and K. Uchida: Jpn. J. Appl. Phys. **36**, 1686 (1997).

[2] S. Amakawa, H. Majima, H. Fukui, M. Fujishima, and K. Hoh, IEICE Trans. Electron **E81-C**, 21 (1998). M. Fujishima, S. Amakawa, and K. Hoh, Jpn. J. Appl. Phys. **37**, 1478 (1998).

[3] M. Kirihara and K. Taniguchi, Abst. of IWCE-5, FrP3 (1997). M. Kirihara and K. Taniguchi, IEICE Trans. Electron **E81-C**, 57 (1998).

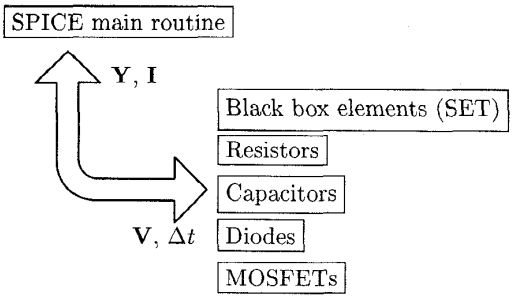

Figure 1: Schematic illustration of electrical parameters exchanged among a SPICE main routine and device elements including black box elements.

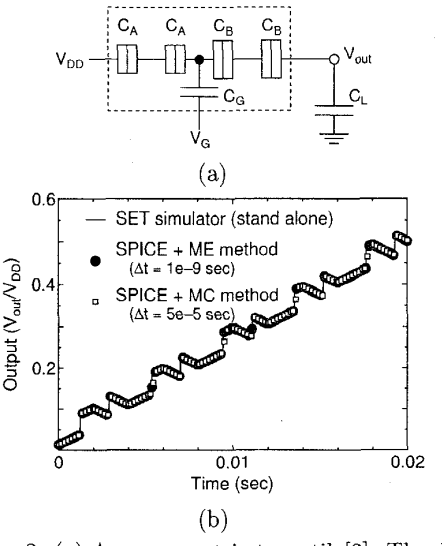

Figure 2: (a) An asymmetric turnstile[3]. The dotted rectangle represents a black box element used in the hybrid simulator. (b) Output characteristics of an asymmetric turnstile simulated at $T = 0.1$K and $C_L = 10e/V_{DD}$. Total CPU times are 42 minutes and 2 seconds for the calculations based on the ME and the MC method, respectively.

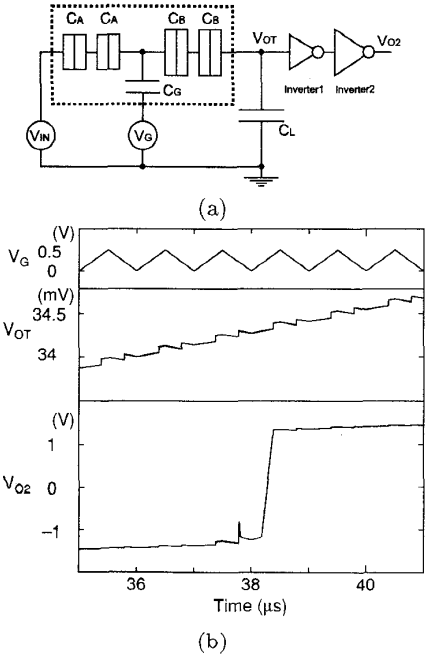

Figure 3: (a) SET counter circuit[3] employing an asymmetric turnstile. (b) The calculated output waveforms calculated using the hybrid simulator based on a ME method at $T = 0.1$K. $V_{IN} = 0.1$V. $C_L = 1$fF. The device parameters of the turnstile are $C_A = 0.801$aF, $C_B = 1.335$aF, $C_G = 0.267$aF. The parameters of the MOSFETs are $t_{ox} = 10$nm, $V_{T0} = -0.70V$(pMOS), $0.75V$(nMOS), Inverter 1: $L = 0.1\mu$m, $W_p = 0.3\mu$m, $W_n = 0.1\mu$m, Inverter 2: $L = 0.1\mu$m, $W_p = 6\mu$m, $W_n = 2\mu$m.