Simulation of high-speed single-electron memory

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1. Introduction

Present one-transistor/one-capacitor (1-T) DRAM cell has an inherent drawback of low margins against various noise sources such as data-line noise, alpha-particle errors and leakage currents in the P/N junction. The amount of charge stored on the memory node should be always maintained as much as 500,000e to keep signal-to-noise ratios large enough. This is a serious restriction when the memory cell sizes are continuously scaled down. To overcome this issue, using a gain cell structure is a promising way, in which a memory node is integrated in the gate of FET. A FLASH memory is one of such gain cell structures. Recently, quite a few FLASH-type nano-dot memory cells [1]-[3] have been reported by using nanoscale quantum dots as a memory node. In these cells, a few electrons are injected from the channel into electrically floating nanocrystal dots through the gate oxide layers. Therefore these cells has a rather long data retention time, but, consequently, the write/erase operations are much slower than DRAMs, typically ranging from 10^{-6} to 10^{-3} seconds.

A different approach to realise a single-electron-based gain cell is to use a MTJ (Multiple Tunnel Junction) [4] as a key component. We have recently proposed a new L-SEM (Lateral Single Electron Memory) architecture [5] to achieve high-speed write operations comparable to the conventional DRAMs. In this paper we present numerical analysis of read/write operations of the L-SEM as well as the robustness against the offset charge issue.

2. Multiple Tunnel Junction Cell

In the L-SEM cell (see Fig.1), an in-plane MTJ is integrated into a central memory node of a split-gate sense MOSFET. The write operation is achieved by the electrons tunnelling through the MTJ between the write word electrode and the memory node. The lateral size of the memory node may be chosen of the order of a few tens nanometers to meet the current lithography conditions. Therefore, the memory operation in the L-SEM is achieved by employing Coulomb Blockade due to multiple electrons ranging from a few to one hundred rather than purely one. The memory-cell array consists of one L-SEM device connected to the source and data lines and read word and write word lines as shown in Fig. 2. A full write/read cycle timing diagram for the L-SEM is shown in Fig. 3.

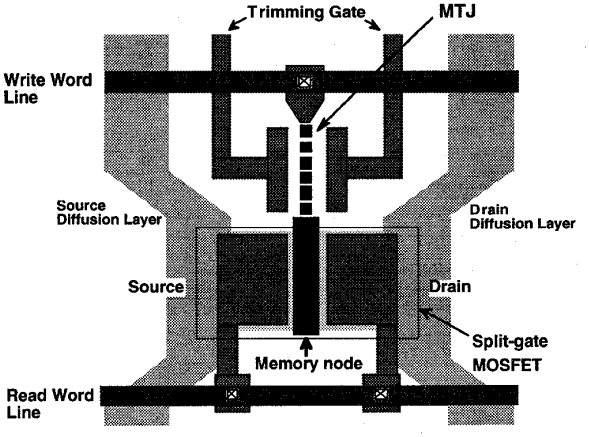

Fig. 1 Lateral Single-Electron Memory (L-SEM) cell layout.

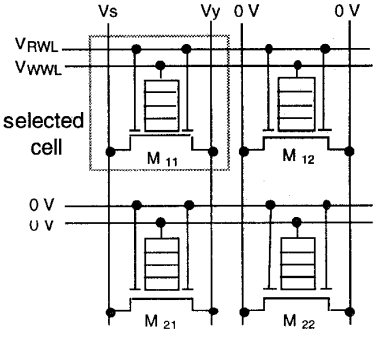

Fig. 2 L-SEM cell array diagram.

The L-SEM cell structure with the MTJ has several advantages. Firstly, it enables larger tunnelling currents, resulting in faster charging/discharging operations. Secondly, the use of the MTJ suppresses the leakage current due to the co-tunnelling. Thirdly, the offset charge effects which are more or less inevitable in practical devices may be reduced.

To design the L-SEM cell structure two-dimensional capacitance simulations were first performed to obtain all the capacitance matrix elements. The size of the central memory node was chosen typically to be 50 nm x 100 nm which can be fabricated by using the electron beam lithography. For simplicity, islands in the MTJs were assumed to be squares with sizes from 2 nm to 5 nm. The number of the islands in

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the MTJs was chosen to be seven which is large enough to suppress the co-tunnelling and is also a typical number achieved in gated heavily-doped silicon nanowires.

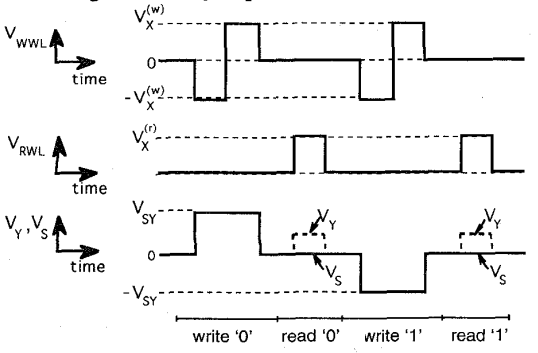

Fig. 3 Schematic write/read cycle timing diagram for the L-SEM.

The obtained capacitance parameters were transferred to an equivalent circuit model for the L-SEM shown in Fig. 4. A single-electron Monte Carlo circuit analysis simulator [6] was used for this study. First, the I-V characteristics of the MTJ were simulated to estimate the Coulomb gap which is necessary to determine V_{WWL} for the writing process.

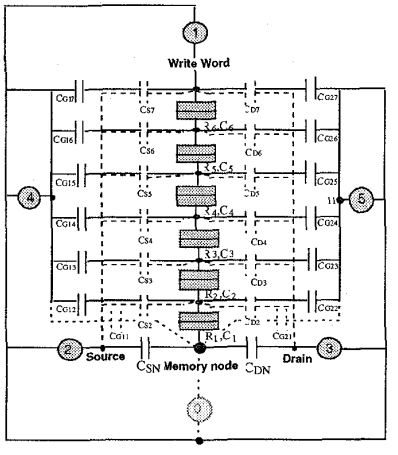

Fig. 4 An equivalent circuit model for the L-SEM cell.

The simulated write word voltage dependence of the current through the MTJ are shown in Fig. 5(a) for two different values of trimming gate bias. Because of the Coulomb blockade oscillation (Fig. 5(b)), the Coulomb gap may be altered by tuning the trimming gate bias.

Full memory sequences were then simulated by performing the transient waveform analysis. When the voltage sequence for the writing process (see Fig. 3) is applied, the L-SEM shows node voltage hysteresis as shown in Fig, 6. The simulation was done at 4.2K for the L-SEM for zero trimming gate bias. For writing '0' (right-hand side of Fig. 6), Vs = Vy = Vsy = 0.1 V is first applied to the source and drain lines. Then a negative word voltage V_{WWL} of -0.12 V is applied to the write word line for injecting

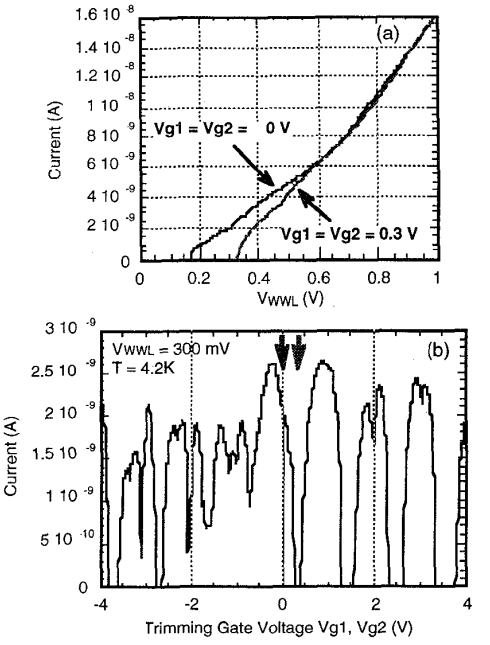

Fig. 5 (a) I-V_{WWL} and (b)I-Vg characteristics simulated for the MTJ with 5-nm islands.

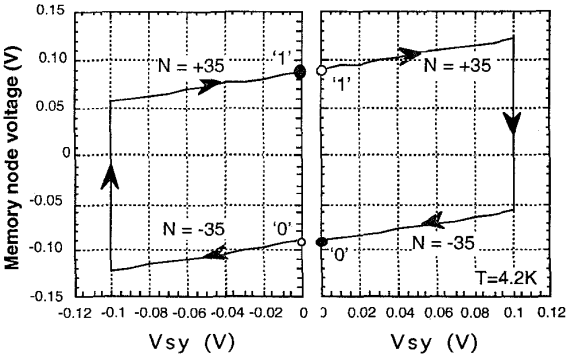

Fig. 6 The hysteresis loop of the node voltage as a function of Vsy simulated for the L-SEM with 5-nm-island MTJ.

electrons into the memory node. After a positive write word line voltage V_{WWL} of 0.12 V is applied, the source and drain line voltages are finally turned off to zero, and the operation point moves to the final state '0'. For writing '1' (left-hand side of Fig. 6), Vs = Vy = Vsy = - 0.1 V is first applied to both the source and drain electrodes, and other sequences are the same as those for writing '0'. The upper and lower branches of the hysteresis correspond to +35e (the absence of 35 electrons) and -35e (the presence of 35 electrons) charge states.

3. High-Speed Write Operation

Transient memory node voltages were next investigated to evaluate the write time of the L-SEM. Figure 7 (a) shows

the cycle timing diagrams used for simulating write '0' and '1' processes. The resulting time-dependence of the memory node voltage and the corresponding number of electrons stored on the memory node are shown in Fig. 7(b). In this simulation Vsy and V_{WWL} were chosen to be 100 and 150 mV, respectively. Fast switching is achieved between high and low levels with a switching time as short as 10 nsec. Details of discretised charging/discharging steps can be seen in Fig. 7(b).

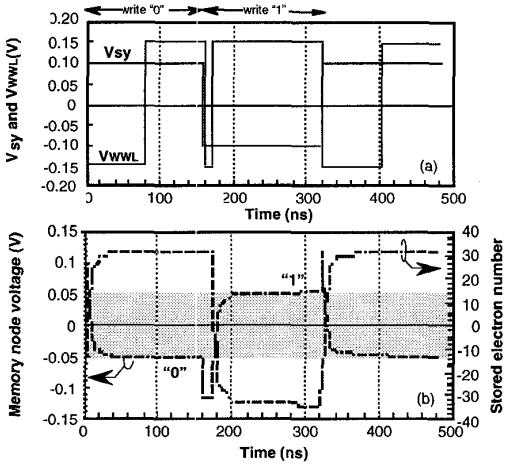

Fig. 7 (a) Write cycle timing diagram for Vsy and V_{WWL} and (b) transient memory node voltage and electron number stored on the memory node.

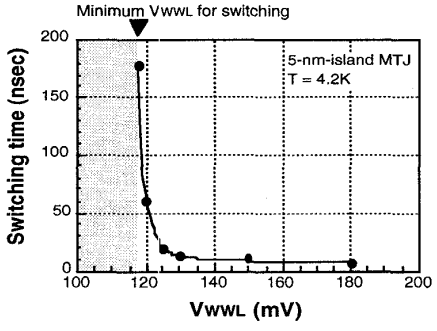

Fig. 8 Switching time as a function of V_{WWL} simulated for the L-SEM with 5x5-nm^2-island MTJ at 4.2K.

We investigated the effects of the word voltage pulse height on these write operations. In Fig. 8, the switching time t_{THL} is plotted as a function of V_{WWL}. The switching occurs above a certain threshold voltage and then t_{THL} decreases rapidly. This is because a larger V_{WWL} results in a larger tunnelling current through the MTJ, leading to faster charging-up. t_{THL} finally approaches the limit determined by $C_\Sigma R_t$. It can be seen that t_{THL} can be reduced to less than 10 nsec for the present 5-nm-islands L-SEM cell structure.

4. Analysis of Sense Characteristics

In the L-SEM, stored memory node voltage V_{node} is sensed by a split-gate MOSFET (see Fig. 1). In Fig. 1, the two gates besides the central memory node act as switch transistors to connect the memory node to the data line. This sense transistor structure enables us to select a particular row of the memory array by applying read word voltage V_{RWL} without disturbing the stored data. To select one particular cell, V_{RWL} is chosen to be 1.0 V while, for other unselected cells, V_{RWL} is kept at 0 V. As we have seen in Sec. 3, the voltage interval between the high and low levels is as small as 100 mV, and so good

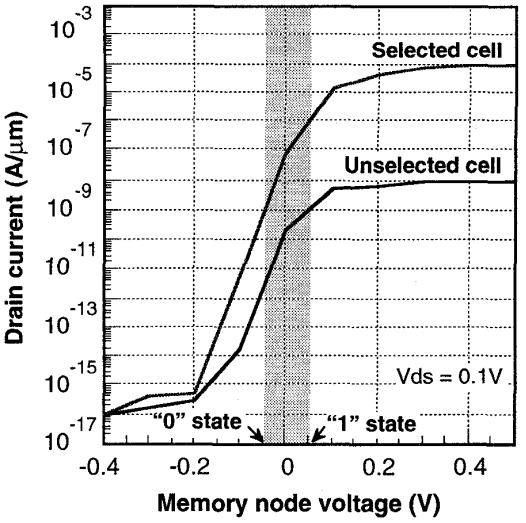

Fig. 9 I_{ds}-V_{node} characteristics of the split-gate sense MOSFET for selected (V_{RWL} = 1 V) and unselected (V_{RWL} = 0 V) cells at 77K. The memory node size and the gap between the memory node and switching gates are 60 nm and 40 nm, respectively.

subthreshold characteristics are required for the sense transistor. The memory node voltage dependence of the drain current of the split-gate MOSFET was analysed by using 2D drift-diffusion device simulation to optimise the split-gate structure. Figure 9 shows the V_{node} dependence of the drain current, Ids, simulated both for selected and unselected cells. The gap length between the memory node and the switching gate is 40 nm and the memory node size is assumed to be 60 nm. It can be seen that the change in the node voltage from -50 mV ('0' state) to 50 mV ('1' state) leads to an increase in Ids from 1 nA/μm to 1 μA/μm, which is large enough to be detected by standard sense amplifiers.

5. Discussion on Offset Charge Effects

Finally, we discuss the offset charge effects in the L-SEM cell. Charged defects at silicon/oxide interfaces are more or less inevitable in the real device structures, which may cause serious effects on the memory operations. From the stand-point of memory design, the most crucial effect of

the offset charge is uncontrollable change in the critical voltage [7]. A density of interface defects achieved in recent silicon process technologies is typically of the order of 10^{10} cm^{-2}, which results in only a few defects per one MTJ area. As long as the offset charge is induced by those few defects, the offset charges on the islands of the MTJ are not random but there should be a certain correlation among them (see Fig. 10). To study these correlated fractional charge effects, we introduced a single charged defect into the L-SEM cell and simulated the I-V characteristics by moving the defect around the MTJ. In the single-electron Monte Carlo simulation, the defect is simply modelled as an extra floating node with a single negative charge on it.

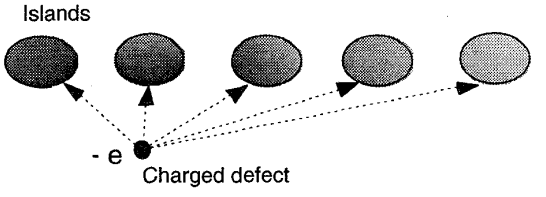

Fig. 10 Schematic diagram of correlated fractional background charge on the islands induced by a single defect charge.

The upper and lower critical voltages were taken from the simulated I-V characteristics, and the data were analysed in a statistical manner as shown in Fig. 11: (a) lower and (b) upper critical voltage distributions. The entire distributions of the critical voltages look like a Poisson distribution with a main peak which is a little below the original critical voltages, ± 0.2 V. It should be noted that no finite probability is seen around zero critical voltage in the distributions. This means that blockade state is always maintained independent of defect positions. This is because many of the tunnel junctions in the MTJ can act to provide a

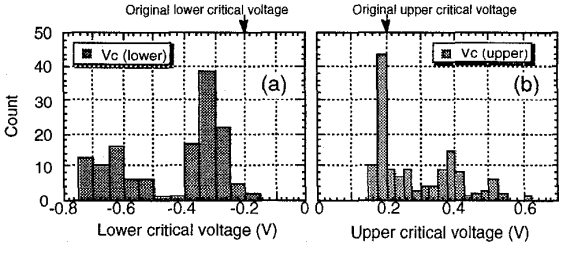

Fig. 11 Distribution of the upper and lower critical voltages induced by a single defect charge.

good blockade even though some of the tunnel junctions close to the defect are broken. In addition, a well defined main peak in the distribution still enables us to design the memory circuits in the same manner as that for an ideal system. This is indeed a big advantage of the MTJ compared with a single tunnel junction in which the blockade is determined only by one tunnel junction. Therefore, as long as the number of the charged defects in one cell is kept smaller than the number of the tunnel junction in the MTJ, the L-SEM structure is robust for offset charge problems.

6. Conclusion

Novel L-SEM architecture and its high-speed write operation were demonstrated with a write time comparable to the conventional DRAMs. Excellent subthreshold characteristics of the sense MOSFET with the split gates were also presented. The robustness of the L-SEM cell structure was also discussed in terms of the offset charge issue.

Acknowledgment

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