PARALLEL IMPLEMENTATION OF A GAAS MESFET ELECTRO-THERMAL SIMULATION ON A TRANSPUTER-BASED SYSTEM

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ABSTRACT

The numerical simulation of a GaAs MESFET device on a transputer-based parallel system is presented. The physical modelling consists of a comprehensive two-dimensional energy transport model taking into account thermal heating effects within the device lattice. The semiconductor equations were solved by an SOR point iterative method using a finite difference discretisation scheme. Algorithms targeted at message passing Multiple-Instructions Multiple-Data (MIMD) distributed memory architectures are described. The efficiency and stability of the parallel algorithms are briefly discussed. A parallel speed-up of 14.3 was obtained on an array of 16 transputers.

1. INTRODUCTION

Semiconductor simulation is a very important tool in the design and understanding of new semiconductor devices. However, the use of accurate physical models usually requires expensive high performance computing resources. The recent advances in parallel processing technology offer a cheap and scalable alternative computing solution. However, parallel algorithms are still needed to complement these systems. This paper presents the parallel numerical simulation of the characterisation of an n-channel MESFET semiconductor device using a time-dependent SOR iterative method. Parallel algorithms for this type of iterative solver were designed specifically for a message-passing MIMD distributed memory transputer architecture. The simulation used a comprehensive electro-thermal MESFET model and the numerical solution was achieved with the finite difference discretisation scheme.

2. THE GAAS MESFET ELECTRO-THERMAL MODEL

The electro-thermal model used in this work is based on an *Energy Transport* model [1] coupled with a *Thermal* model [2]. This comprehensive model accounts for hot carriers effects and the influence of lattice heating on the electron flow not included in the standard *Drift-Diffusion Transport* model. A *Scharfetter-Gummel* formulation for current density and energy flux was used. The governing equations for the MESFET device are as follows:

Poisson
$$\nabla^2\psi = -\frac{q}{\varepsilon_o\varepsilon_r}(N_D - n) \tag{1}$$

Current Continuity
$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla\cdot\boldsymbol{J}_n + G \tag{2}$$

Current Density
$$\boldsymbol{J}_n = q\mu_n(w_n)n\boldsymbol{E} + q\boldsymbol{D}_n(w_n)\nabla n \tag{3}$$

Energy Density Conservation
$$\frac{\partial W_n}{\partial n} = \boldsymbol{J}_n\cdot\boldsymbol{E} - \nabla\cdot\boldsymbol{S}_n - \frac{W_n - W_{no}}{\tau_{w_n}(w_n)} \tag{4}$$

Energy Flux
$$\boldsymbol{S}_n = -\mu_n(w_n)n\boldsymbol{E} + q\boldsymbol{D}_n(w_n)\nabla W_n \tag{5}$$

Thermal
$$\nabla\cdot(k_L\nabla T_L) + H_S = 0 \tag{6}$$

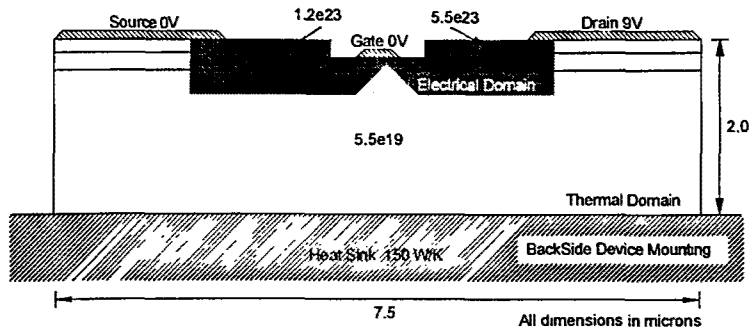
Heat Generation
$$H_s = q\frac{W_n - W_{no}}{\tau_{w_n}(w_n)} \tag{7}$$

where $\psi, N_D, n, t, J_n, G, \mu_n, E, D_n$ are, respectively, the potential, donor density, electron concentration, time, current density, recombination, mobility, electric field, diffusion coefficient, $W_n, S_n, W_{no}, \tau_{w_n}$ are, electron energy flux, energy density, equilibrium energy flux, energy relaxation time and k_L, T_L, H_s are lattice thermal conductivity, lattice temperature, heat generation respectively.

3. TIME-DEPENDENT NUMERICAL ALGORITHM

The numerical solution is achieved using a finite difference discretisation scheme. The semiconductor equations consisting of the closely coupled Poisson, continuity and energy equations are solved by a Gauss-Seidel point iteration method with successive relaxation for a time-dependent solution [3].

The thermal model couples with the carrier transport model to form a coupled electro-thermal model. The solution of this model is obtained by sequentially solving the Poisson (1), current continuity (2) and energy density conservation (4) partial differential equations once per time-step. This time-stepping process is repeated until a steady state solution is reached. The elliptic thermal equation (6) is also solved with the SOR technique but for steady state conditions as the lattice temperature usually remains constant at the DC bias condition [2]. The lattice temperature is therefore solved at regular intervals in the time stepping process, i.e. for a total simulation time of 2.5ps, for time-steps of 5fs, the thermal equation is solved every 0.25ps and the new lattice temperature obtained is subsequently used.



Low Field Mobility = 0.8 m^2Vs^{-1} Gate Width = 400e-6 m

Figure 1. Generic Power GaAs MESFET Device

The thermal boundary has been restricted to the same domain as the carrier transport equations, therefore equivalent third-order boundary conditions are required. To obtain accurate results, the domain for analysis has to be extended horizontally for 2 to 3 times the source-drain spacing and to a depth of 5 to 10 times the active region of the device [2]. Instead of solving the equation over the electrical domain (i.e. 3.5 by 0.5 microns - greyed) a much wider thermal domain (i.e. 7.5 by 2.0 microns - white) has to be solved as depicted in Figure 1. As a result, more computational resources both in memory and processor time are needed to solve the device problem This is naturally suited to a scalable parallel system.

4. PARALLEL ALGORITHMS & IMPLEMENTATION

The parallel system used consists of an array of TRAnsputer Modules (TRAMs) connected in a ring network topology. Each TRAM has a transputer and some local memory. The device simulation problem has been parallelised using a one dimensional geometric domain decomposition [4] as shown in Figure 2. A sub-domain of the whole MESFET is locally stored on each TRAM's memory and each transputer computes the solution of its sub-domain concurrently.

The finite difference discretisation of the semiconductor equations results in a five-point discretisation scheme. This requires some communication of boundary data between neighbouring processes. The efficient design of communication protocols is very important in a parallel environment. The aim is to minimise communication overheads.

The two main overheads are attributed to the *control* and *data exchange* protocol. The *control* protocol is based on a driver-slave principle. The driver sends messages via the control channel to the slaves to perform specific tasks. The iterative nature of the numerical algorithms requires messages from all the slaves to the driver so that the latter can test for the convergence of solution across the whole domain. The *data exchange* communication protocol ensures data consistency across boundaries between neighbouring processes. The algorithm communicates data via the exchange channels (refer to Figure 2).

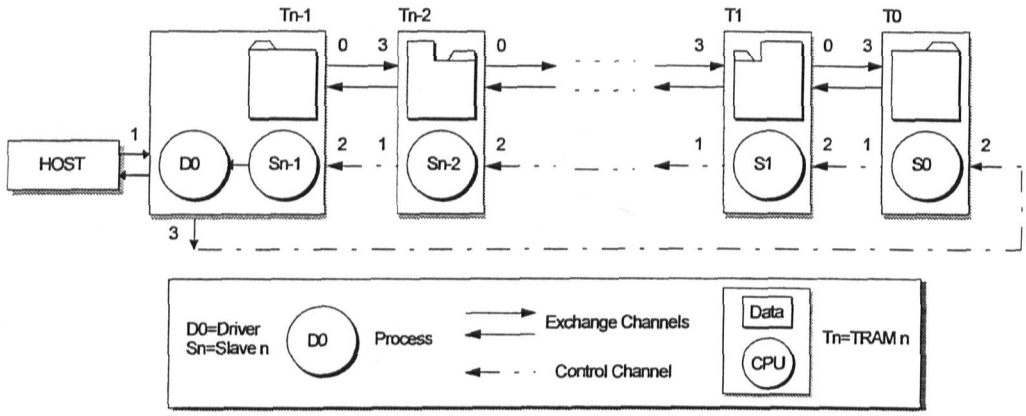


Figure 2. Configuration and Mapping of Simulation on an Array of TRAMs (n=16)

The convergence of the iterative solution requires a modified red/black checker-board one-dimensional partitioning method named as the *RB 1D SOR* [5]. This parallel ordering method is essential for the optimum convergence of the point iterative scheme.

5. RESULTS AND PERFORMANCE

Simulation and system performance results were obtained from the parallel system by simulating the recessed-gate GaAs MESFET depicted in Figure 1 using a uniform grid for the bias condition shown. Figure 3 shows the electron and lattice temperature profiles of the GaAs MESFET device.

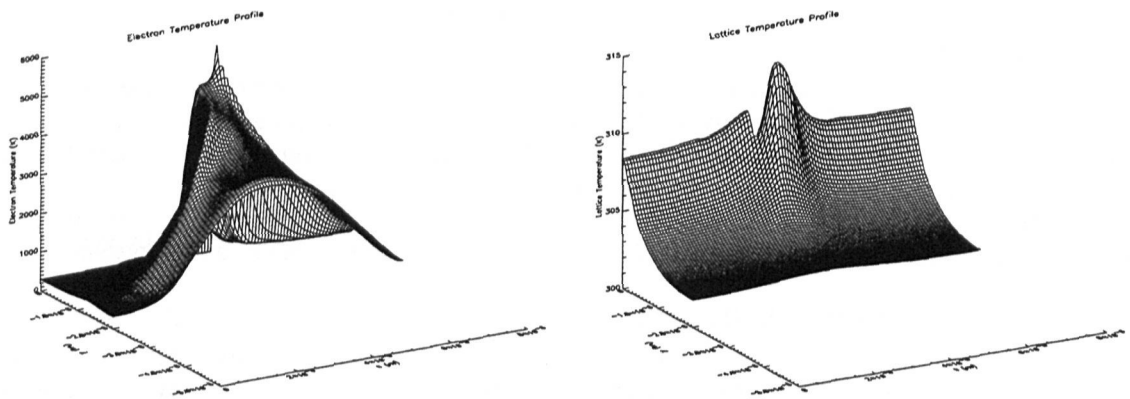


Figure 3. Electron and Lattice Temperature of GaAs MESFET device

Although the parallel simulator was shown to performed adaptive meshing efficiently[5] for an electrical model, the electro-thermal simulation has been restricted to a uniform grid of 96x60 owing to memory limitations on the TRAMs. Table 1 shows the performance of the parallel system, solving the full electro-thermal equations iteratively using the *RB 1D SOR* partitioning method, with the solution computed over a time of 2.5ps (500 time steps of 5fs) for steady state solution.

The numerical solution for this particular problem converges in roughly the same number of iterations when simulated on the parallel system. Using a single transputer, it took about 6.5 hours to compute that solution but only about 0.5 hour with 16 transputers.

Nodes	Iteration Number				Time
	Poisson	Current	Energy	Thermal	(hr)
1	21380	2718	2061	491	6h36
4	21351	2718	2062	492	1h43
8	21324	2659	2042	492	0h53
12	21295	2716	2058	492	0h36
16	21256	2709	2060	491	0h28

Table 1. Performance of the Parallel Simulation

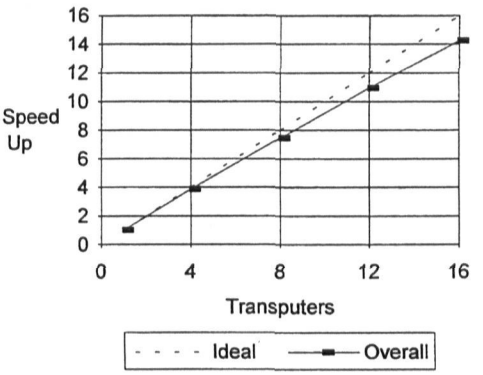


Figure 4. Overall Parallel Performance

As shown in Figure 4 a speed increase of up to a factor of 14.3 on 16 transputers is possible with the current algorithm. The drop in performance for large number of transputers is attributed to the increase in the communication to computation ratio due to a fix domain size. Increasing the size of the problem as the number of processors is usually recommended for efficient use of parallelism. Otherwise most time is spent on communication of data rather than useful computation as is the case for very small domains.

6. CONCLUSION

A complete parallel numerical simulator for the characterisation of a GaAs MESFET device has been presented. Geometric domain decomposition was the natural way of parallelising the problem enabling a logical map on a distributed memory system. In addition to the numerical algorithms, efficient parallel algorithms are required to manage the communications protocols in this distributed-data environment. We found that careful implementation of the communication protocols is important to achieve high parallel efficiencies. A modified red/black partitioning updating method is also required to provide optimum convergence. The Gauss-Seidel point iterative method with successive relaxation was very suitable for parallel implementation. An advantage of this method is that the inclusion of additional equations such as the energy density conservation and thermal equations follow the same parallel principle that is used for Poisson and current continuity equations. The parallel methods developed and implemented in this work proved that parallel processing is a feasible computing alternative that can be used to provide fast characterisation of semiconductor devices.

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