AN ALTERNATIVE METHOD FOR COMPACT MODEL CONSTRUCTION AND PARAMETER EXTRACTION

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ABSTRACT

The conventional method to extract circuit parameters from device simulators is through I-V and C-V curve-fitting on a presumed device model, whose basic form is often analytically derived using drift-diffusion equations with space-charge-region approximation. The resulting device model is usually either too simple to reflect detailed device behaviors or too complex that most of its internal parameters are rule-of-thumb fitting factors. In consideration of the device simulation level, the profile information on dopings and physical quantities is mostly lost after fitting of only the terminal characteristics. In this paper, we implement an alternative methodology for linking the device and circuit simulators based on the lumped-element (LE) model [1] and a new compiler-based circuit simulation environment [2]. Since the device model is not hard-wired, we show that a more flexible tradeoff between accuracy, predictivity and efficiency may be obtained.

I. INTRODUCTION

Compact device models used in circuit simulation remain as the base of the electronic CAD design system, since it is the first abstraction level beyond the spatial coordinates. Yet compact models were less useful in consideration of predictive designs during technology evolution owing to many nonphysical fittings for the purpose of accuracy. In recent years as the computational resources become more powerful and accessible, technology CAD tools and environment have grown mature on their usage and calibration in the device level. However, on a typical module level with 500 to 10,000 transistors), TCAD tools, even though they can be presumed as very accurate and predictive (for a summary of TCAD limitations and recent developments, see [3]), are still too expensive even in any scale. Hence, the abstraction step toward compact models must be applied. Traditionally, parameter extraction for compact models is based on optimal fit of IV or CV data obtained from lab measurements or simulated TCAD terminal characteristics (see [4-6] for examples). The compact model usually has different levels of complexity, but within each level the circuit linkage is hard-wired. For the most complex level, the physical meaning of each element is often sacrificed for fitting accuracy. This procedure will also lose most of the insight and sensitivity of the detailed profile information provided by the TCAD simulations. Therefore, we choose to implement another method for compact model construction and parameter extraction, which can have flexible configuration inside the model and utilize the profile information from TCAD to construct its parameters. This method can be conveniently implemented in compiler-based circuit simulation environment [2]. We will demonstrate the procedure by a transient study of a 1-D $n+-p$ junction diode [7].

II. The LUMP-ELEMENT METHOD

The lumped-element (LE) method (sometime called the equivalent-circuit method) [1] has been proposed more than three decades ago as an alternative representation of the drift-diffusion (DD) and generation-recombination (G-R) mechanisms inside a device besides the partial-differential

equations (PDE) representation. In LE, the device is partitioned to charge elements, and within the element, the fluxes (J_n the electron, J_p the hole and J_D the displacement currents) are connected with charge storage elements and current sources representing the time derivative of carrier concentrations and G-R, while the continuity equation becomes Kirchhoff's Current Law (KCL) in the newly constructed equivalent circut. If every spatial node in the PDE scheme corresponds to a dual charge element, these two representations can be regarded as equivalent. Nearly all of today's device simulators [3], however, employ the PDE scheme for discretization owing to its better and more convenient numerical properties (such as the Scharfetter-Gummel scheme and tight relations to computational geometry). Nevertheless, for construction of compact models, LE offers very important and direct physical insight. It has been shown that the one-lump model of the bipolar transistor is analogous to the Ebers-Moll model [1]. Moreover, it has been demonstrated that by including the geometrically distributed effects, the compact model can be more flexible and accurate [8]. Yet, the number of lump levels to account for distributed effects can be kept very small [9].

Based on these observations, we implement the LE scheme *only at* the parameter extraction step. Given the solution profiles from device simulators, a more flexible and physically transparent compact model can be constructed accordingly. For a simple example of an $n^+ - p$ junction diode, the compact model can be extracted to optimally fit the IV and CV data (the conventional method, see Fig. 1) or can be constructed so that each element corresponds to some profile variation (the LE method, see Fig. 2). The resistors are identified with variations in potential while the carrier concentrations are almost constant and net charge trivial. The junction capacitor is identified with a net immobile charge dipole, and the diffusion capacitor is identified with a surplus of minority carriers. The values of these circuit elements are bias (or state) dependent (nonlinear resistors and capacitors, current sources and charge-storage elements), and advanced circuit simulators which provide two-terminal table-lookup and nonlinear parameter calculations can take these inputs with little extra efforts [2, 7, 10].

Below we will demonstrate the LE scheme for transient analyis step by step on the 1-D $n+-p$ junction diode. The material parameters and device structure is chosen arbitarily to minimize computational efforts and confusion (such as the device is much longer than the minority carrier diffusion length, simplified doping profiles and physical models in device simulation, etc.). The diode is first simulated with steady-state device simulators. The device states at reverse bias, close to and at equilibrium, at subthreshold and at heavy injection are recorded and analyzed. The charge profiles and corresponding model elements for reverse bias and heavy injection states are shown in Figs. 3-5, respectively. When the circuit element is not necessary at certain state (for instance, the diffusion capacitance at the reverse bias), it is simply given a trivial value in the nonlinear table lookup entry. For detailed analyses on junction operations that can be predicted by device simulators, see [11]. Fig. 6 shows the transient simulation results using the device simulator, the best-fit scheme and the present LE scheme.

III. ANALYSIS

Our approach has the following advantages over the conventional method of parameter extraction using optimal fitting:

1. the linkage and the number of circuit elements is not hard-wired. Since the contours of equal potentials or concentrations become circuit nodes in the new compact model and the tradeoff between accuracy and efficiency can be readily made. Exact accuracy of the device simulator can be obtained by constructing the full node-to-element LE scheme. However, the compu-

tational efforts to achieve acceptable accuracy should be much smaller than full LE (most of the important electronic mechanisms happen at a small portion of the entire device), and much smaller than the PDE scheme using smart-grid adaptation where Steiner points from grid construction can be surplus due to the geometrical constraints.

2. the error in device simulation parameters (such as mobility) can be directly reflected on the circuit element parameters (such as resistance). The errors from the abstraction steps and from the input parameters of device simulation can be easily separated. In comparison with parameters extraction based on the optimal fit of IV and CV data, statistical analysis and worst-case estimation on process variations can be performed more efficiently. Also, since the abstraction over the spatial coordinates has been solely performed in one step, the concept of statistical metrology [12] for manufacturing becomes clear.
3. since the optimal fitting of all element parameters on lumped terminal IV and CV data is never invoked, advanced (and hence time-consuming) numerical algorithms like numerical annealing to find multiple local minimum are not necessary.
4. the circuit elements are physically transparent. The improvement of compact models can be done in an automatic, evolutionary way, based on the the progress of the device simulation.

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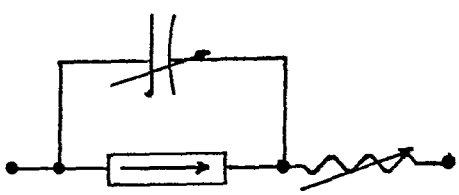

Fig. 1. Compact model of a p-n diode for the optimal-fit method.

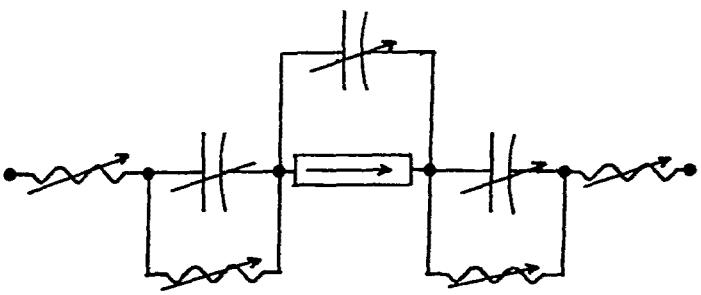

Fig. 2. Compact model of a p-n diode for the equivalent-circuit method. ρ is the net charge.

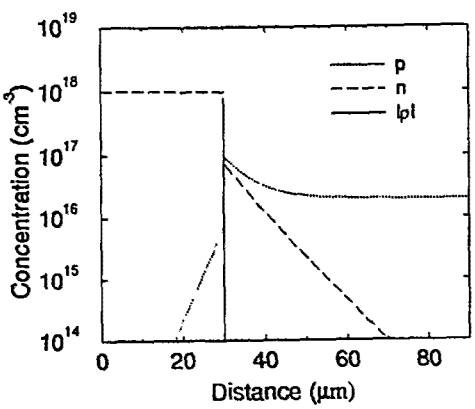

Fig. 3. The concentration profiles at a high-injection state of an $n^+ - p$ diode.

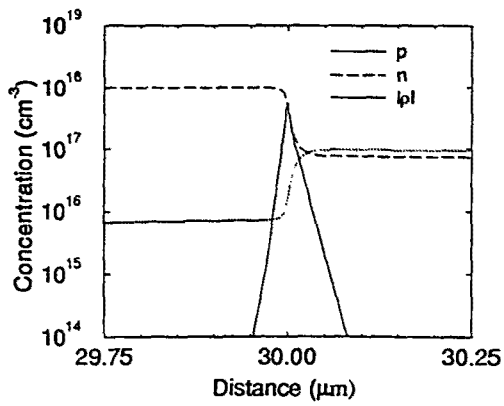

Fig. 4. The junction magnification of Fig. 3. The abrupt junction is at 30 μm.

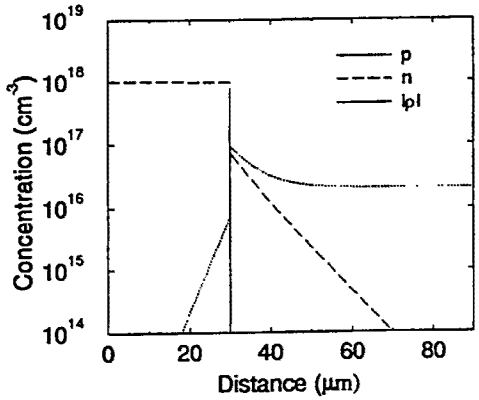

Fig. 5. The concentration profiles at a reverse-bias state.

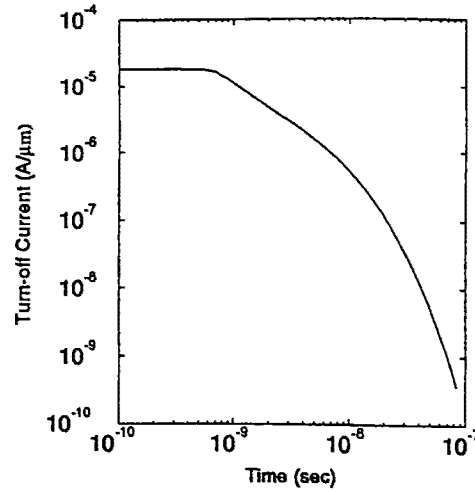

Fig. 6. Transient analysis of switching from the high-injection state to the reverse-bias state.

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