APPLICATION OF HIERARCHICAL TRANSPORT MODELS FOR THE STUDY OF DEEP SUBMICRON SILICON N-MOSFETS

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Abstract

In this paper, we present an integrated tool set with a hierarchy of transport models ranging from the drift-diffusion (DD), through various hydrodynamic(HD) to Monte Carlo (MC) models. Good agreement is achieved between experimental long-channel n-MOSFET drain current data and simulations using the DD, HD, and MC models. The MC simulator is also applied to the study of transport in deep submicron, silicon n-MOSFETs with special attention given to issues related to power supply scaling.

I. INTRODUCTION

Moment-based simulators based on drift-diffusion (DD) and hydrodynamic (HD) formalisms provide tools for device design and research. It is widely recognized that these formalisms do not account for all phenomena of importance to deep submicron device performance. A more complete and physical, but expensive, description of the device behavior can be obtained from Monte Carlo (MC) simulations. While carefully tuned DD simulators do a remarkably good job of predicting device terminal characteristics, especially for longer channel MOSFETs, HD and MC simulators offer deeper insights useful for the design of deep submicron MOSFETs.

In this paper, we analyze the effects of scaling channel length and power supply on device reliability and drive using our HD and MC simulators. Two nMOS transistors with effective channel lengths of 0.13 and 0.08 μm and realistic doping profiles are considered.

II. MOMENT-BASED SIMULATORS

The two-dimensional MOSFET simulator includes a hierarchy of transport models ranging from the traditional DD, a parabolic and a non-parabolic HD [1], an energy transport model and the HD model proposed by Stettler *et al.* [2]. The hierarchical implementation is embedded within the device simulator MINIMOS 5.2 [3]. A unified,, robust and efficient discretization method was used to discretize the hierarchical HD models. We have also extended the field-dependent mobility model of Shin *et al.* [4] to HD applications by replacing the local longitudinal electric field with an "effective" field obtained from the full band MC energy versus field relation. Each of the HD models is cast into a generalized form allowing a uniform numerical discretization for all models. A specific HD model is selected by choosing the values of H, η, R_1, and R_2 [1]:

Current Flow:

$$J = \mu nE + \mu HT\nabla n + \mu n(1+\eta)\nabla(HT) \quad (1)$$

Energy Flow:

$$S = -\tfrac{5}{2}R_1 JT - \tfrac{5}{2}R_2(n\mu T)\nabla T \quad (2)$$

III. MONTE CARLO SIMULATOR

The Monte Carlo simulator is based on SLAPSHOT [5], a tool that uses analytic fits to the pseudopotential bandstructure of silicon. Advanced features of SLAPSHOT include a scattering rate computation based on the pseudopotential bandstructure and a detailed calculation of the impact ionization rate based on an anisotropic energy threshold. Ionized impurity scattering, acoustic intra- and inter-valley phonon scattering and optical phonon scattering are included. The impact ionization strength was tuned to give good agreement with the experimental ionization rates in bulk silicon [5]. Surface scattering is included via surface roughness and interface fixed charge scattering [6]. Additionally, the transport kernel in the MC device simulator has two windows for repetition in real space

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and one in the energy domain. Convergence to a self-consistent solution is obtained through iterations with a non-linear Poisson solver.

IV MODEL DEVELOPMENT AND VALIDATION

An important application of our MC simulator has been in the development of our HD model. Quantities such as the relaxation time, field dependence of the average energy and velocity, amount of heat flux have all been determined using SLAPSHOT. As pointed out by Ramaswamy *et al.* [7], MC plays a significant role in verifying the contributions of the various quantities in the HD equations.

The different models in the hierarchy of device simulators will have to demonstrate reasonable agreement in the device characteristics with experimental data for long channel MOSFETs (with smoothly varying lateral fields) before they can be used to study deep submicron MOSFETs. Drain current calculations were performed with all three simulators for a range of drain and gate biases for two different sources of devices. The first device is an LDD MOSFET with an effective channel length of 0.48 microns. As seen from Figure 1, surface scattering plays a significant role in decreasing the drain current in the linear region. However, its role is quite small in the saturation region. The second device is a single drain MOSFET with an effective channel length of 0.32 microns. The agreement with the experimental data is very good (Figs. 1 and 2) and suggests cautious optimism in the use of the HD and MC simulators for shorter channel lengths. This agreement is partly due to the work that has gone into describing surface scattering in the HD and MC codes. Also, recent work by Ramaswamy *et al.* [7] suggests, once again, the utility of our nonparabolic HD model. In the remainder of this work, "HD model" refers to our nonparabolic HD model.

V. CHANNEL LENGTH AND POWER SUPPLY SCALING

HD and MC simulations were performed on two test structures with effective channel lengths of 0.13 and 0.08 microns. These are representative channel lengths for future MOSFET technologies. The devices are single drain MOSFETs with a junction depth of 40 nm, oxide thickness of 5 nm and a step-like channel doping. We looked at single drain MOSFETs to ascertain if they offer reasonably good device performance. We were also interested in device performance at these dimensions under worst case conditions. The doping at the surface (mid to high 10^{17} cm^{-3}) was adjusted to obtain good turn-off characteristics (threshold voltage of 0.5 V in saturation for both the channel lengths) and a deep implant (low 10^{18} cm^{-3}) was included to minimize punchthrough.

For constant lateral fields, shorter channel lengths have shown higher reliability (lower substrate current) [8]. However, operation at peak substrate current can determine the lifetime of a device and is hence of great interest. For this reason gate voltages that maximized substrate current at a given drain bias (power supply) and channel length were chosen.

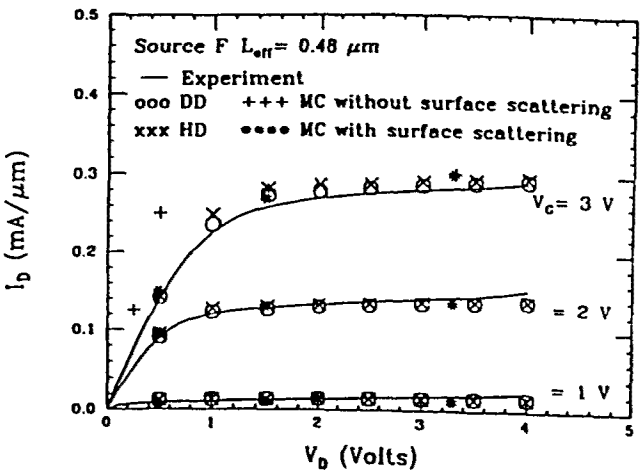

Figure 1: Comparison of the I_D vs V_D characteristics as simulated by the DD, HD and MC tools with experimental data for the device with L_{eff}=0.48 microns.

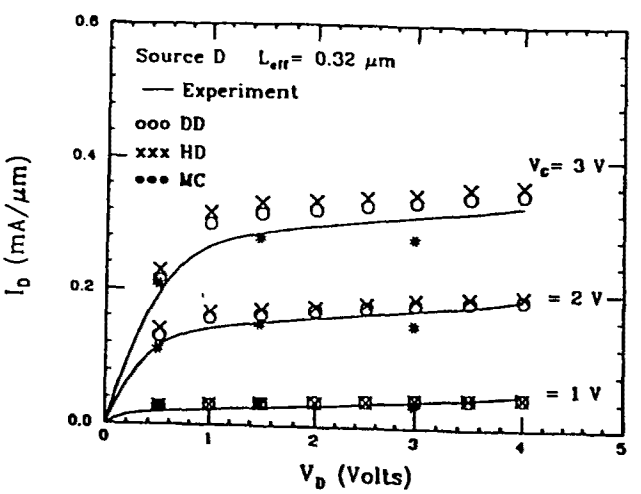

Figure 2: Comparison of the I_D vs V_D characteristics as simulated by the DD, HD and MC tools with experimental data for the device with L_{eff} = 0.32 microns.

VI. RELIABILITY

Substrate current is an index of the amount of impact ionization in a device. Impact ionization degrades threshold voltage, transconductance and affects oxide integrity through electron trapping in the oxide and at the interface. The energy distributions of the carriers provide information on the amount of hot carriers in the device. The average electron distributions are shown in Figures 3 and 4 respectively for the two drain voltages. Even though the two channel lengths exhibit similar distributions in energy, the distribution at about 1.4 eV (where impact ionization takes place) is much higher for the 2.5 V case (and higher for the shorterchannel length). Also, please refer to Figure 5 for a plot showing the average electron energies (from both HD and MC simulations) in the channel. This suggests a much higher substrate current with 2.5 V on the drain.

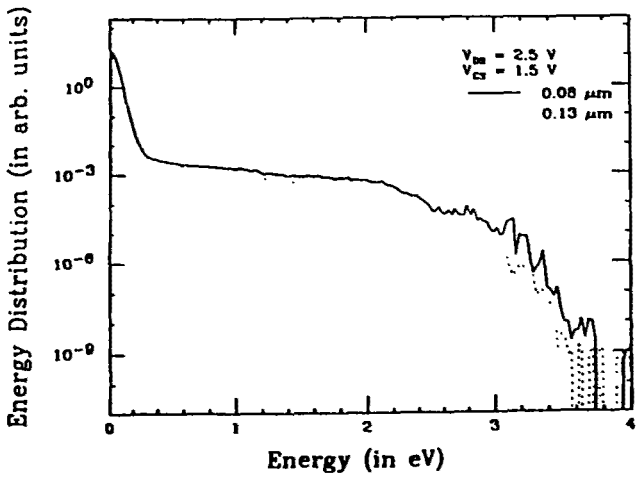

Figure 3: The electron distributions with 2.5 V on the drain and 1.5 V on the gate for channel lengths of 0.08 microns (solid line) and 0.13 microns (dots).

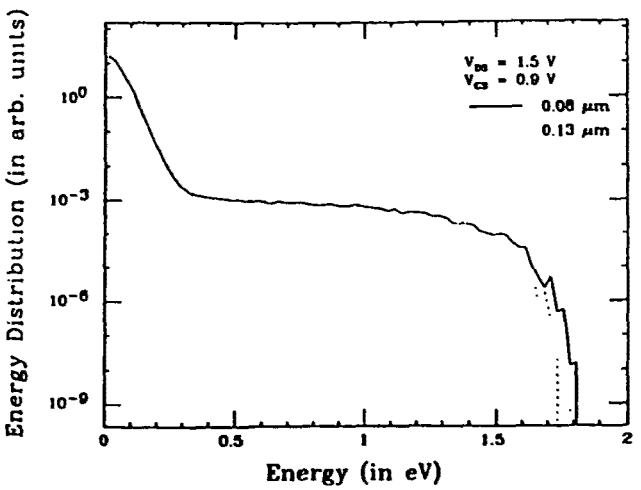

Figure 4: The electron distributions with 1.5 V on the drain and 0.9 V on the gate for channel lengths of 0.08 microns (solid line) and 0.13 microns(dots).

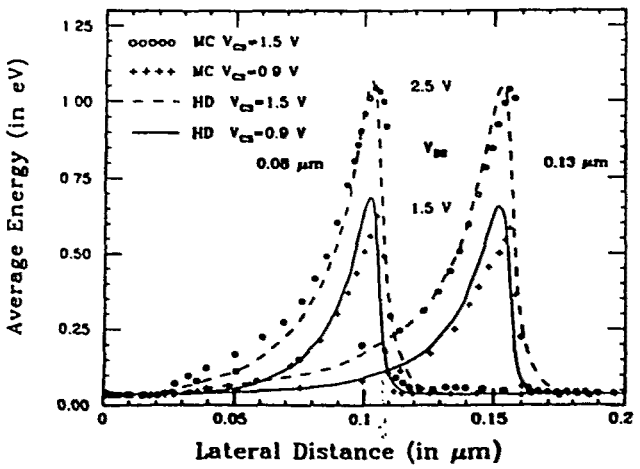

Figure 5: Average electron energies with HD and MC models: 1.5 V on the drain and 0.9 V on the gate for channel lengths of 0.08 microns (solid line) and 0.13 microns (dashes); 2.5 V on the drain and 1.5 V on the gate for channel lengths of 0.08 microns (dots) and 0.13 microns (dots and dashes). Symbols are used for the MC data.

Contrary to the observed dependencies of substrate current on channel lengths for constant field cases, we observe that substrate current increases with a decrease in the channel length when operation at peak substrate current is considered. This supports previous studies [9] which predicted continued degradation of device lifetime with channel length scaling at sub 0.2micron channel lengths. However, as expected, the dependence of substrate current on the drain bias (power supply) is much greater than on the channel length (more so as we get close to the threshold for impact ionization).

Despite the increasing role of interconnects on the overall circuit delay, device speed is still an important issue. The larger the drive current the faster the charge transfer and hence the circuit speed. The drain currents in the two devices were obtained to be 0.23 and 0.3 mA/micron respectively from MC simulations for the 2.5 V case, while for the 1.5 V case, the drain currents in the two devices were 0.07 and 0.09 mA/micron respectively. The average lateral velocities obtained from MC simulations are shown in Fig. 6. Velocity overshoot is comparable over the two channel lengths and drain biases, but the drain currents themselves are

different. This is due to the differences in the velocities before the overshoot (closer to the source). It is interesting to note that the overshoot is actually smaller with 2.5 V on the drain. This is probably due to the fact that average energies are larger with 2.5 V on the drain (as compared to the 1.5 V case) (resulting in increased scattering).

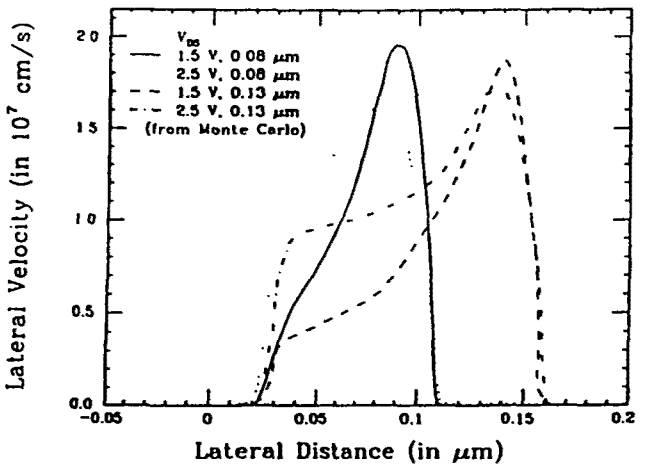

Figure 6: Average lateral velocities with: 1.5 V on the drain and 0.9 V on the gate for channel lengths of 0.08 microns (solid line) and 0.13 microns (dashes); 2.5 V on the drain and 1.5 V on the gate for channel lengths of 0.08 microns (dots) and 0.13 microns (dots and dashes).

It is evident that scaling to sub 0.1 micron channel lengths should be accompanied by a decrease in the power supply. Also, further scaling at sub 0.1 micron channel lengths leads to limited gains in the drive current and negligible increase in the hot carrier degradation. The biggest drawback with scaling the power supply is the decrease in the drive current. A decrease in power dissipation is an added benefit of decreasing the power supply. As long as the device speed is a significant factor determining the overall circuit speed, serious attention must be paid to maximizing the drive current as well. Different structures and/or doping profiles can be investigated for this purpose. The above discussion suggests that a trade-off between drive and substrate currents can be achieved by choosing a suitable power supply with or without additional device design.

VII. SUMMARY

In this paper, we presented an application of a hierarchy of transport models ranging from the drift-diffusion to the Monte Carlo. We demonstrated good agreement between the experimental drain current data and our simulations for devices from two different sources with channel lengths of 0.32 and 0.48 microns. Using this agreement as a first test of model validity, we applied the MC tool to test devices with channel lengths of 0.13 and 0.08 microns. Some issues related to power supply voltage selection such as its effect on device reliability and drive current were highlighted.

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