THREE-DIMENSIONAL SIMULATION OF THE EFFECT OF RANDOM IMPURITY DISTRIBUTIONS ON CONDUCTANCE FOR DEEP SUBMICRON DEVICES

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Abstract

We present a 3-D simulation of small semiconductor devices, investigating the random impurity fluctuation and distribution effect on the conductance. Instead of using a uniform background charge for the impurities, discrete charges are assigned atomistically to computing cells by checking the assigned random numbers generated by computer, so that the scheme satisfies that the requirement that the mean value of the total discrete charge equals that of the uniform doping. The simulation is performed for MESFET structures. The random impurity distribution effect on devices with gate lengths less than 0.1 μm and narrow width will cause non-negligible conductance variations and be a major source of device variability within a single chip.

I. INTRODUCTION

In general, semiconductor device operation depends on the use of electrical potential barriers (such as gate depletion) in control of the carrier (electrons and holes) transport through the devices, in order to achieve signal switching and signal modulation. Although a successful device design is quite complicated and involves many aspects, the device engineering is mostly to devise a "best" device design by defining optimal device structures and manipulating impurity profiles to obtain optimal control of the carrier flow though the device. This becomes increasingly difficult as the device scale becomes smaller and smaller. New problems keep hindering the high performance requirement. Well-known problems include hot carrier effects, short-channel effects, etc. We discuss a potential problem caused by impurity fluctuation [1] which can not be perfectly controlled by the device engineer as devices become too small, and intend to provide better understanding of its effect on device design requirement for small devices.

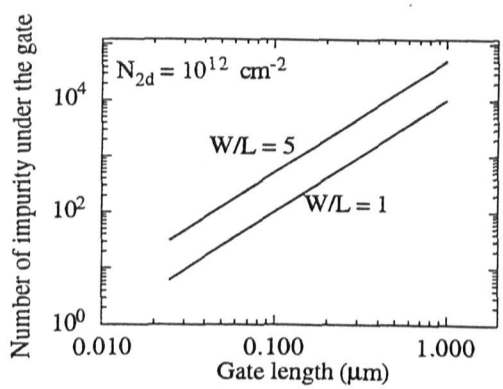

Fig. 1 Number of electrons under the gate versus gate length (L) for two gate width (W) to gate length ratio.

Impurities in semiconductor devices are randomly distributed as a result of the nature of processing, such as ion implantation. Although electron transport in the devices always experiences

*Work supported by the Army Research Office.

the effect of the random distribution of the impurities, the statistical contribution of these effects to the electronic performance of devices with a large operation domain (in space dimension, such as volume in which electrons flow) is negligible, and a simplified uniform background impurity distribution (the average of the impurity charges in space) is adequate in describing the effect of the fixed charges in the devices. Only devices with a small active domain which is susceptible to a large percentage fluctuation of the impurities, will exhibit noticeable conductance variations. For device scaling to the deep submicron regime, especially for device feature size less than 0.1 μm, as shown in Fig. 1, the number of impurity under the gate will approach the hundreds level and several tens of dopant number level. When the active device region contains so few dopant atoms that the statistical fluctuation of the dopant is comparable to the dopant number itself, the dopant fluctuation, either in total number and/or in spatial distribution, in the device will cause non-negligible effects on device performance. The anticipated effects include the classical statistical effects such as the device current level shift and threshold voltage shift due to the total dopant number fluctuation and/or distribution. Only a few attempts have been devoted to study the effect of random atomistic impurity on device performance, with the most recently reported research [3] using a drift-diffusion model to simulate the random impurity effect on sub-0.1 μm MOSFET devices. We investigate the classical effects from the simulation of a 3-dimensional device structures for MESFET by using hydrodynamic equations, with the discrete 3-dimensional random impurity distribution and fluctuation included.

II. DEVICE SIMULATION

The device structure considered is a 3-D volume as depicted in Fig. 2, which shows the contact definitions and a possible impurity distribution. The discrete impurity region is defined only in the highly doped layer away from the simulation domain boundary (smooth uniform doping is used at the contact ends) in order to use the existing simulation program and avoid dealing with very complicated rough-boundary conditions for the time being. This treatment should not affect the simulation results since most of the active device region (the channel) is well inside the discrete impurity distribution region and device operation is dominated by the electron transport through this region. The charge in a discrete cell is set to be either one or zero following a distribution scheme. The corresponding uniform doping in the highly doped layer is 1.5×10^{18} cm^{-3}. In sampling of 5000 devices, we plot the frequency as a function of dopant number under the gate in Fig. 3, which has a mean value at 36 (approximately one tenth of the mean value for the total discrete impurities in the device, since the volume of the gate region is one tenth of the volume of the total discrete region), with a standard deviation of 5.99.

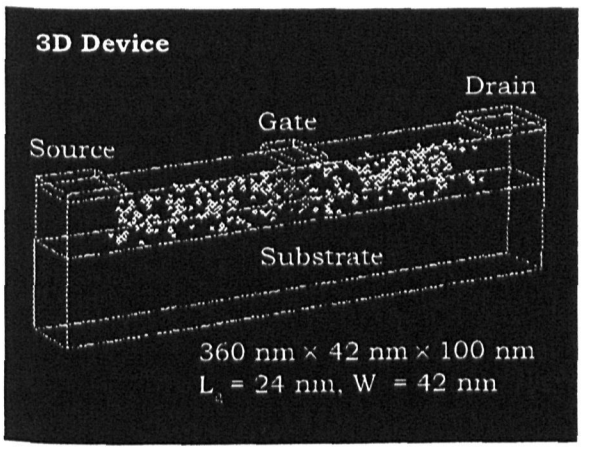

Fig. 2 A 3D device model and computer simulated discrete impurity distribution.

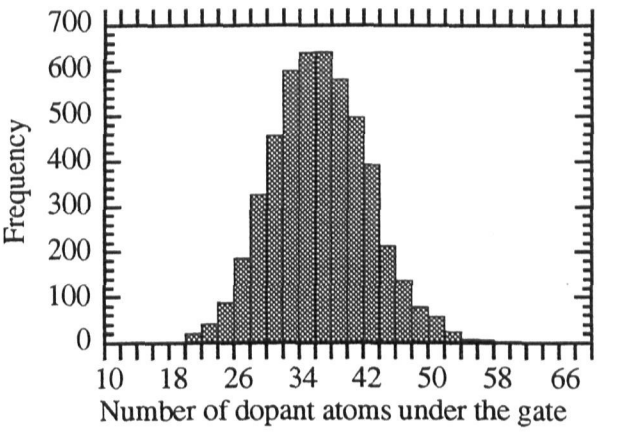

Fig. 3 Statistical frequency as a function of the number of impurity under the gate for 5000 devices.

The simulation domain is discretized into uniform small volume cells of 3 nm × 3 nm × 3 nm, and various physical quantities are computed for these small cells. The device simulation method is the same as that used in [4], which numerically solves a set of hydrodynamic equations that describe the conservation of particle, momentum and energy of electrons, in conjunction with Poisson's equation, using a finite-difference algorithm.

III. SIMULATION RESULTS

The simulated device structure (Fig. 2) is a domain of 0.36 μm (L) × 0.1 μm (H) × W, with W in the range of 0.042 μm to 0.162 μm. The thickness of the highly-doped layer is 40 nm, and results for two different gate lengths are discussed here. In Fig. 4, we plot the drain current versus gate voltage for three different MESFETs, where the drain potential is 0.5 V in all cases. One may notice that for the 24 nm gate devices, the current increase is not linearly proportional to the device width, as one would expect for the uniform doping case. Since there is no narrow width effect included in this simulation, and the number of impurity under the gate is 24 and 56 for W = 42 and W = 60 (more than doubled for the later case), respectively, the deviation from the expected behavior is apparently due to the impurity fluctuation and distribution in the devices. It is worth while to point out that the total impurity for the entire discrete region is not doubled: 358 for W = 42 and 610 for W = 60, respectively.

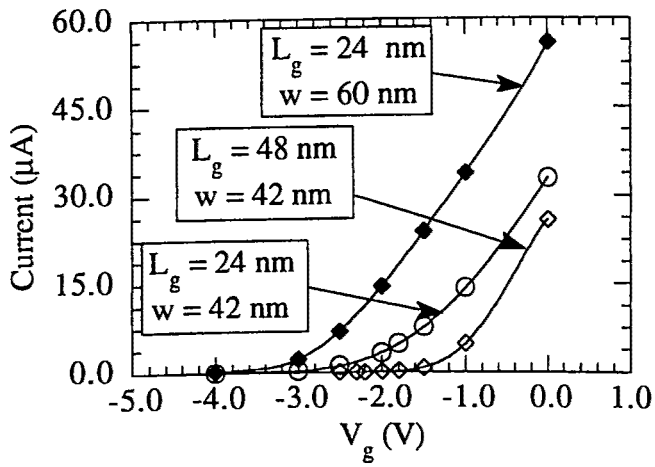

Fig. 4 I-V_g characteristics of MESFETs for three different gate cases, for V_d = 0.5 V.

The current fluctuation, caused by the variation in random impurity distribution and fluctuation, is pronounced for the device geometry simulated here. In Fig. 5 and Fig. 6, we plot the drain current as a function of gate voltage and drain voltage, respectively, for different number of impurities under the gate. Two characteristics are obvious. First, the total dopant fluctuation under the gate causes significant current variations. Secondly, it's not necessarily that more impurity under the gate will definitely cause more current flow, one can see the numbers are not ordered in both figures. This means that not only the number of impurities under the gate is important, but also the actual positions of the impurities. In Fig. 5, the current difference becomes wider as the gate bias becomes more negative. This is expected since the number of impurities in the opening channel becomes smaller as the depletion under the gate becomes wider, thus the fluctuation increases until the channel is completely depleted. For comparison, in Fig. 6, the results of simulation with uniform background doping is also included. Obviously, the current levels with discrete impurities fluctuates the current level of the uniform doping. The simulation shows that the variations can be as large as 30 per cent for the particular MESFET device structure.

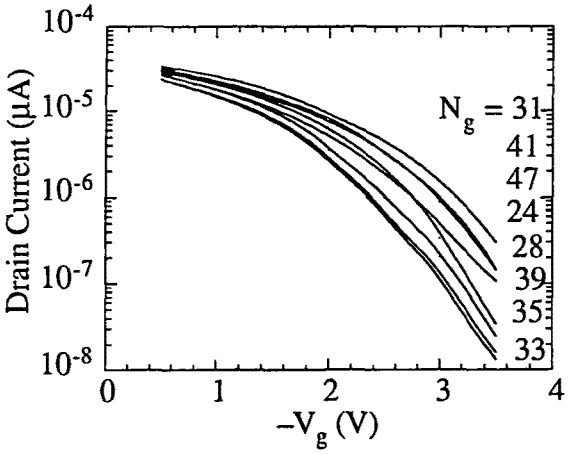

Fig. 5 I-V characteristics of gate voltage for a 24 nm gate MESFET, showing the current fluctuation as the impurity fluctuate under the gate.

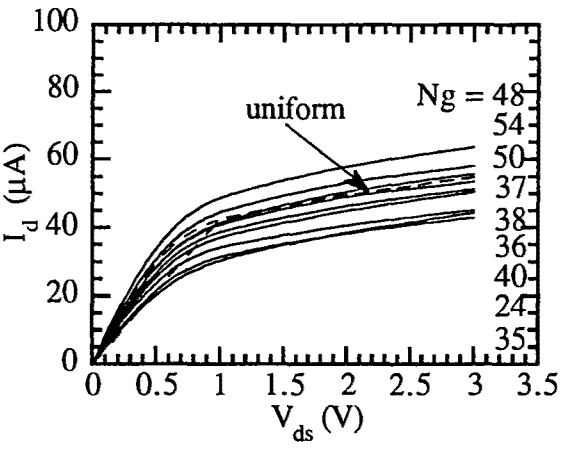

Fig. 6 I-V characteristics of drain voltage for a 24 nm gate MESFET, showing the current fluctuation as the impurity fluctuate under the gate.

We emphasize here that the current fluctuation mainly depends on the fluctuation and the distribution of the impurities under the gate, by inspecting the relation of the current fluctuation and the total dopant in the whole discrete region, we find that the current variation doesn't follow the total dopant fluctuation in the discrete dopant region clearly. This means that the impurity fluctuation in the whole device region is much less critical to the current flow through the channel, compared to the influence of the impurities under the gate. This is as expected, since the critical region that determines the current flow is the region under the gate, and also the impurity fluctuation and distribution under the gate are essentially independent of that of the whole device region.

IV. CONCLUSION

We investigated the effect of random impurity fluctuation and distribution on small device operations. For the device structure simulated here, the results suggest that the effects of random impurity fluctuation and distribution can cause large current variation for small devices if the total gate area is very small. As we expected, from our simulation, the random impurity effect on the device performance will be reduced with increase of the gate length or gate width. But the effect could be effective, even for a device with gate length close to 0.1 μm. A wider gate length device will be helpful in suppression of the effect of random impurity fluctuation. A full 3-D simulation of the device including the random impurity effect for engineering application may not be practical. We think that a combination of limited 3-D simulation plus statistical method might be needed in providing an applicable method to estimate the random impurity effect on device performance for device down scaling to 0.1 μm range.

References

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