Monte Carlo Modelling of Sub-Micron Delta-Doped MOSFETs

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Abstract

A 2D multilayer MOSFET simulator has been developed, using self-consistently coupled ensemble Monte Carlo and 2D Finite Element Poisson Solver algorithms. The simulator is used to investigate the operation of sub-micron delta-doped MOSFETs, in order to assess their suitability for high density logic applications. An operating window is observed within which the delta-doped devices exhibit a significant reduction in surface carrier density, relative to conventional MOSFETs, implying reduced surface scattering and gate injection.

I. Introduction

In order to achieve Ultra Large Scale Integration (ULSI) densities in CMOS, the gate lengths of silicon MOSFETs must be reduced well below 1μm. It is well known that sub-micron MOSFETs are prone to a number of short channel effects: increased lateral electric fields result in enhanced hot carrier generation, whilst increased vertical fields pull carriers hard onto the Si/SiO_2 interface - leading to increased interface scattering and hot carrier injection into the SiO_2 layer. The latter effect results in an accumulation of trapped charge in the oxide, which causes eventual device failure by shifting the threshold voltage and reducing the ability of the gate to modulate charge.

These problems may be alleviated by using a delta doped MOSFET structure [1,2], in which conduction occurs, not at the Si/SiO_2 surface, but in an ultrathin, highly doped layer located typically 200-400Å below the interface. Thus, both interface scattering and hot carrier injection should be reduced: however, realistic modelling work is necessary to determine the efficacy of the delta layer in confining carriers, its effect on the surface carrier density and energy distribution, and the extent of any consequent reduction in hot carrier degradation.

In this paper, we describe the development of a 2D self-consistent Monte Carlo simulator, and its application to modelling electronic transport in delta-doped MOSFETs. In very short gate devices transport can no longer be described in terms of steady state mobilities and saturation velocities, and the traditional drift-diffusion approach to device modelling becomes inadequate. The Monte Carlo method is well established as a powerful technique for modelling highly non-equilibrium transport phenomena, and can yield a detailed microscopic insight into the operation of semiconductor devices. The initial investigation presented here concerns the basic issues of transistor operation and carrier distribution in short gate delta doped MOSFETs, and the effect of the delta-doped layer on the surface electron density.

II. The Simulation Program

We have developed a high specification 2D simulation program for sub-micron multilayer MOSFETs. The program consists of an ensemble Monte Carlo algorithm self-consistently coupled to a 2D Finite element Poisson Solver. The 2D Poisson equation is re-solved every 1fs: such a short timestep is necessary to avoid undersampling of the plasma oscillations which occur in the highly doped source and drain implants of silicon MOSFETs.

The Finite Element mesh can be defined by the user, but is restricted to a rectangular grid format. This restriction greatly simplifies the determination of the 2D charge density in the device from the distribution of Monte Carlo particles. The ability to specify non-uniform mesh spacings is essential for both delta-doped and conventional MOSFETs, in order that the potential at, in the former case, the delta-doped layer, and, in the latter case, the surface inversion layer, may be accurately modelled.

Electronic transport in the MOSFETs is modelled using a nonparabolic, ellipsoidal description of the 6 silicon X-valleys Intervalley, and acoustic intravalley phonon scattering is included using the parameter set recommended by Brunetti et al.[3], which was found to produce good agreement with experimental drift velocity data. Impurity scattering is included via the Brooks-Herring model.

The effect of degeneracy (Pauli exclusion) is modelled using the approach described by Lugli and Ferry [4], in which the probability that an electron is scattered into a state of energy E is weighted by 1-f(E), where f(E) is the local electronic distribution function. In our simulation, the distribution function may be sampled in up to 8 different spatial regions - including the source and drain implants, and sections along user defined surface and buried layers - to account for spatial variations in electron density and carrier heating.

In order to model self-consistently the electrostatic potential at the pn junctions between the implants and the channel region, a 2D hole density is included in a zero current (fixed quasi Fermi level) approximation, as described by Fischetti and Laux [5]. A damping scheme is employed to ensure a smooth convergence to the fixed quasi Fermi level condition. The effect of the hole density on the electrostatic potential is particularly important for very short gate devices, where the acceptor density must be increased in order to combat drain induced barrier lowering and punchthrough.

A particle replication scheme [6] is utilised to increase the sampling capability of the simulator in the channel region of the devices. For a replication factor M, any particle entering the channel region is replicated M-1 times. Particles attempting to enter an implant region are annihilated with a probability (M-1)/M. Correspondingly, all particles in the implant regions have an associated charge M times greater than those in the channel region.

The source-drain current is calculated by summing the x-component of velocity for all particles located between the source and drain implants [7]. This method enables a much larger sample to be used than in the traditional approach of counting particles emitted/injected at the source and drain contacts.

Several authors have modelled surface scattering in MOSFETs by allowing both specular and diffusive reflection of particles which impinge on the oxide interface [8]. Our program allows any proportion of diffusive reflections to be specified; however, for this particular investigation, we have used specular reflections only. The extent of surface scattering is primarily important in determining the relative speed of delta-doped and conventional MOSFETs, an issue which will be the subject of a separate investigation. For the same reason we have not, at this stage, included any sophisticated description of impurity scattering in the delta-doped layer: such refinements may readily be made, as and when required.

The program runs for typically 2-5 hours per bias point on an HP 710 workstation. The actual run time depends on the device size and bias conditions, with simulations of shorter devices generally taking less time. Access to a large networked cluster of workstations at Newcastle means that a simulations for a whole set of bias points can be run in parallel, on the same timescale.

III. Results

We have modelled a 0.1μm delta-doped MOSFET with the following specification. The delta doping dose was $10^{12}cm^{-2}$ - implemented as a 20Å doping plane, with a bulk doping density of $5x10^{18}cm^{-3}$. The delta-doped layer was located 200Å below the Si/SiO_2 interface. A doping density of $2x10^{19}cm^{-3}$ was used for the source and drain implants: whilst this value is lower than those encountered in some MOSFET structures, it was found sufficient to define a flat potential across the implant region - hence providing a suitable model of an ohmic contact. The implant depth was taken as 500Å, and a length of 1000Å of each implant was included in the simulation. Again, this length was found sufficient to model the ohmic contact and the surrounding potential. The use of higher implant doping densities, or the inclusion of a greater length of implant, leads to large increases in CPU time, with no significant gain in physical information or quantitative accuracy.
Short gate MOSFETs can suffer from high leakage currents due to drain induced barrier lowering. The effect can be alleviated by increasing the substrate doping and, in common with previous reports on 0.1μm conventional MOSFETs, we have specified a doping density of $10^{17}cm^{-3}$ for the p-type silicon substrate. Threshold voltage shifts are also a problem in short gate FETs: we have chosen an oxide thickness of 50Å, in order to reduce the gate voltage swing required to turn the device off. Assuming an n-type polysilicon ohmic contact, our simulations predict a threshold voltage of around -1.5V for the device under investigation. Obviously, the threshold voltage varies with the delta layer depth and dose. We have used a drain bias of 1V in our simulations, reflecting the reduced supply voltage anticipated for use in ULSI.

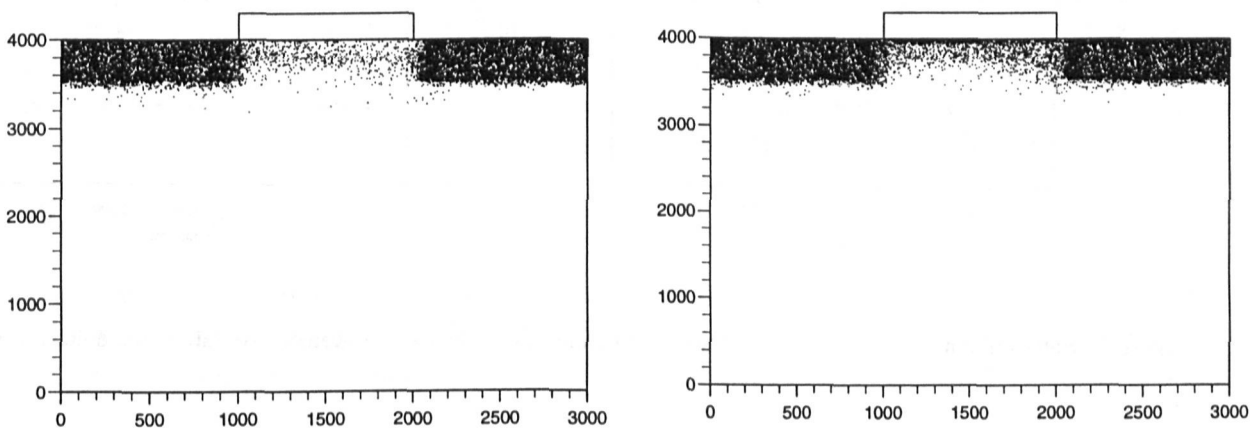

Figure 1. Steady state electron distribution: (a) V_G=0V, V_D=1V (b) V_G=0.75V, V_D=1V

Figures 1(a) and (b) show instantaneous plots of the 2D electron distribution in the device, during steady state operation, for gate biases of 0V and 0.75V. Figure 1(a) shows conduction occurring well below the oxide interface; however, it is clear that the delta layer does not provide strong carrier confinement, with electrons travelling in a very broad current channel. On the other hand, in figure 1(b), for V_G = 0.75V, an inversion layer has formed at the interface; the device is now operating primarily in a surface channel mode. This type of transition has also been observed in drift-diffusion modelling of long channel devices [9].

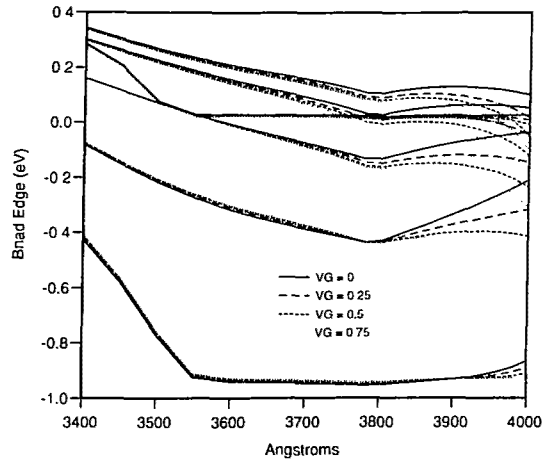

Figure 2. Conduction band edge profile vs. vertical distance, with 4000Å corresponding to the oxide interface. For each gate bias, a set of six 'slices' of the potential profile are shown, taken at 200Å intervals along the channel from souce to drain. The profiles corresponding to the endpoints of the channel are pinned close to the source and drain biases for most of the vertical distance shown, whilst the other four profiles appear in descending order moving along the channel from source to drain.

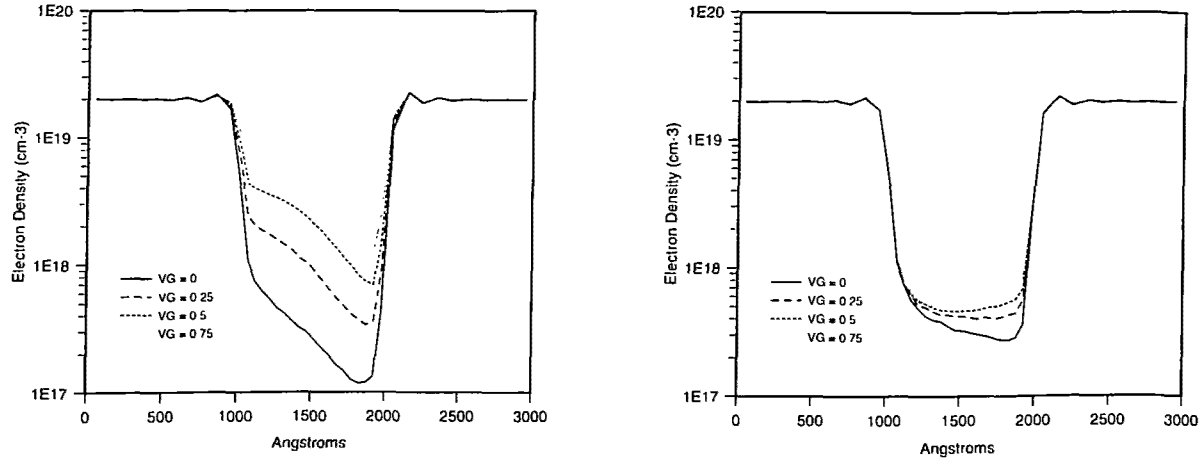

Figure 3. Electron density vs. distance from source to drain: (a) at the oxide interface, (b) along the delta-layer

Figure 2 shows several sets of vertical 1D slices through the conduction band edge profile, for a range of gate biases. In this figure it can be seen that the potential 'notch' caused by the

delta layer is quite shallow and, as the gate bias is increased, the potential at the oxide interface drops below that in the delta layer, along most of the channel length. Figures 3(a) and (b) show the electron density along the surface layer and the delta layer, for the same range of gate biases. Comparing the two figures, it is clear that the surface electron density exceeds the delta layer density for all the gate biases shown except for $V_G = 0$. This conclusion is consistent with the potential profiles shown in figure 2, which also indicate greater surface accumulation for $V_G > 0V$. At $V_G = 0V$ the drain current for this device is 0.21mA per micron gate width. For comparison, we simulated a 0.1μm conventional MOSFET with the same implant, oxide and substrate specification. Approximately the same drain current, 0.21mA/μm, was obtained for a gate bias of 0.3V. In figure 4 we have compared the surface electron densities for the two devices. The surface electron density for the delta doped device is less than one third of that in the conventional MOSFET, for the same drain current. An equal current comparison was also performed for the $V_G = 0.25V$ bias condition on the delta doped device, and a reduction in the surface electron density - by a factor of approximately 2.5 compared to the conventional device - was still found, even though the delta-doped MOSFET showed appreciable surface conduction.

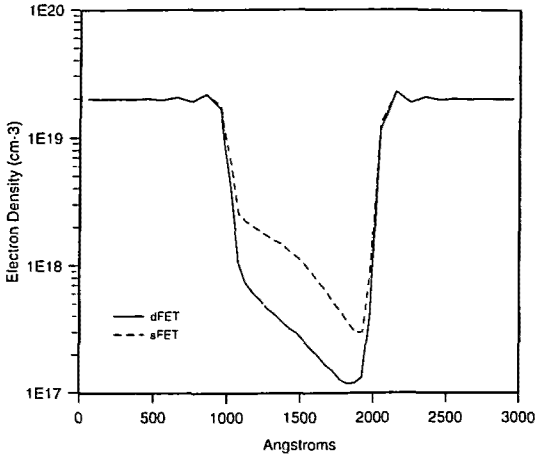

Figure 4. Surface electron density vs. distance from source to drain for a 0.1μm delta doped MOSFET (dFET) and a conventional surface channel device (sFET)

Obviously, a different result may be obtained by varying the depth of the delta-layer below the oxide interface. We have carried out simulations of devices with delta-layer depths of 100Å, which show that the conducting channel spreads up to the oxide interface, even when no surface inversion layer is formed. Conversely, further reductions in surface carrier density may be achieved by increasing the delta-layer depth, but this reduces the transconductance and the threshold voltage: beyond a certain depth, gate control can be lost altogether [9].

IV. Conclusions

We have used a 2D multilayer MOSFET Monte Carlo simulator to investigate the operation of 0.1μm delta-doped MOSFETs. The devices have an operating 'window' of gate biases within which the conducting channel is centred on the delta-doped layer. In this mode, a substantial reduction in the surface carrier density can be obtained, relative to conventional MOSFETs, implying consequent reductions in surface scattering and gate injection. Outside this operating window, a parasitic surface channel is formed, and the above advantages are

diminished. The operating window is large enough to be compatible with logic operation at a reduced supply voltage of 1V.

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