Numerical Simulation of IGBTs at Elevated Temperatures

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Abstract
In this paper we present a 2D finite difference device simulator which has been developed to underpin the design and optimisation of power IGBTs. The simulator has been used to investigate the effect of elevated temperatures on the performance of the IGBT for use in environments where ambient temperatures up to 200°C are likely. The preliminary results of this investigation are reported here.

I. Introduction

The Insulated Gate Bipolar Transistor (IGBT) (Fig.1) is at present one of the most widely used power semiconductor devices [1]. Its popularity among the designers of power electronics systems is due to the lucky combination of a low forward voltage drop, typical for power BJTs, and gate controlled turn-off and high switching speed characteristic of power MOSFETs [2]. At the same time the coupled field effect and bipolar actions make the device operation quite complicated [3].

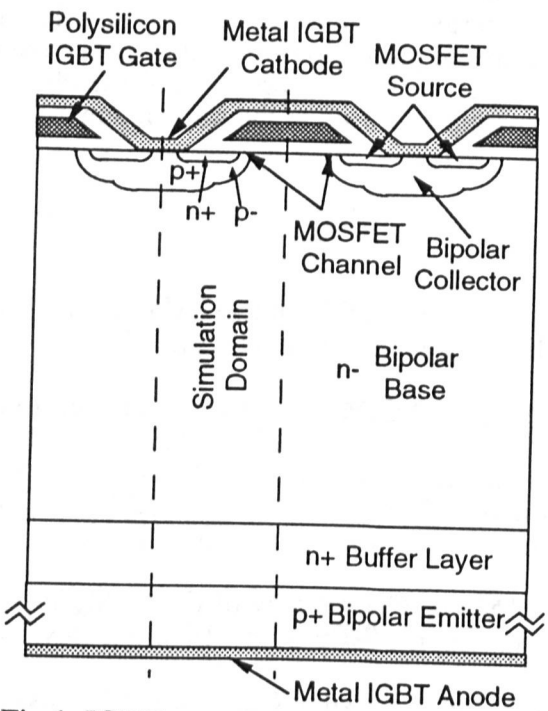

Fig 1. IGBT structure

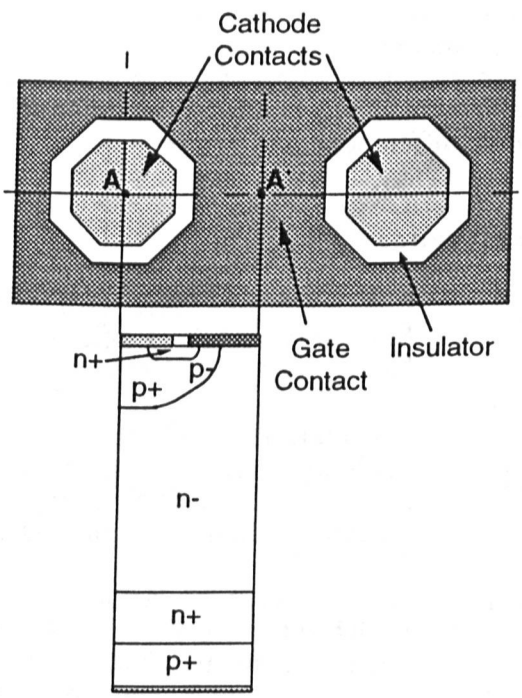

Fig 2. IGBT cell structure and simulation domain

The device behaviour is strongly affected by the cell geometry, MOSFET channel length, actual doping distribution and lifetime killing treatments. The traditional empirical approach to the

device design is inadequate and impractical. It is widely recognised that the device design and optimisation should rely on a proper 2D or even 3D numerical simulation [4]. Although many general purpose simulation packages are now available, they are not usually optimised for the simulation of IGBTs and frequently do this job slowly and unreliably.

Here we report on a new power semiconductor device simulator developed to underpin the design and the optimisation of IGBTs. The simulator have been applied to study the behaviour of relatively short channel IGBTs at high temperatures up to 200°C. Such high temperature operating conditions are typical for the application of these devices in aircraft power conversion systems.

II. The Simulation Program

Our steady state IGBT simuator is based on the solution of the Poisson equation and current continuity equations for electrons and holes. Heavy doping effects are included through bandgap and electron affinity variation in a manner similar to those used for the simulation of compound semiconductor devices. A finite difference method is adopted for discretisation. Although it is well known that the global Newton procedure provides better convergence in the case of strongly coupled equations, a modified Gummel-like iterative scheme is used for nonlinear iterations because it provides a simpler way towards the parallelisation of the simulation code which will be the next step of this development. An appropriate logarithmic dumping for the Poisson equation in combination with a bounded change in electron and hole concentrations [5] ensure convergence in the whole dynamic range of applied on-state voltages up to latch-up conditions. In reverse bias mode the logarithmic dumping provides convergence for the Poisson equation up to several thousand volts. A fast Incomplete LU Factorisation Biconjugate Gradient (ILUBCG) solver is employed for the solution of both Poisson and current continuity equations. The solution time of the three nonlinear equations in the Gummel cycle is significantly reduced if only a few ILUBCG steps follow each nonlinear Newton like step.

In order to simulate properly the high temperature IGBT behaviour appropriate semi-empirical expressions are included for all relevant silicon parameters. The temperature dependent mobility model of Nishida and Sah [6], which includes the scattering mechanisms of surface and bulk acoustical and optical-intervalley phonons, bulk ionised impurities, oxide charges, surface roughness and dipoles or neutral surface states, was modified to account for the carrier-carrier scattering on high injection cases. The recombination terms consist of two components: a Shockley-Read-Hall term and an Auger recombination term. Although slight temperature dependence of the electron and hole lifetimes and Auger coefficient may be expected, due to the lack of relevant data we assume in our analysis that these parameters are temperature independent.

Fig.2. shows an octagonal IGBT cell structure with our solution domain which is a cross section along the line A-A' and which takes into account the symmetry between two neighbouring cells. It is clear however that the 2D simulation is quite a rough approximation to the actual 3D nature of this device and cannot represent cell interaction totally accurately, for example the influence of the distributed parasitic vertical JFET. It is planned to develop a 3D device modeling program implemented on a Parsytec parallel transputer system in order to investigate the effects due to the inherent 3D nature of the device. Additional uncertainty in the results of the simulation is introduced by the approximation for the lateral distribution of the impurities in the MOSFET channel. For a given vertical doping profile (measured using spreading resistance method), experimental results have shown that different assumptions for the lateral impurity distribution can have a marked effect on the subthreshold MOSFET characteristics and the threshold voltage. It is therefore of vital importance when modeling an actual device to have an accurate 2D and in future 3D description of the doping profile, particularly of the channel region, if the results are to give a reliable model of the device characteristics.

III Results

Three typical I_D-V_D curves calculated at room temperature, 100°C and 200°C are given in Fig.3 for V_G=15V which is the expected operating gate voltage for the device. Fig.4. shows a plot of I_D vs V_G for room temperature and 200°C at a drain voltage V_D=2V. Both a logarithmic plot (solid lines, left axis) and a linear plot (dotted lines, right axis) are shown on the same graph. The potential, electron and hole distributions (V_G=15V, V_D=2V) for the top region of the device (to a depth of 15μm) at room temperature and at 200°C are presented in Fig.5(a,b,c) and Fig.6(a,b,c) respectively. Equipotentials are at -0.15V intervals while equi-concentration contours show the power of ten of the concentration, i.e. contour no.16 represents $10^{16}cm^{-3}$

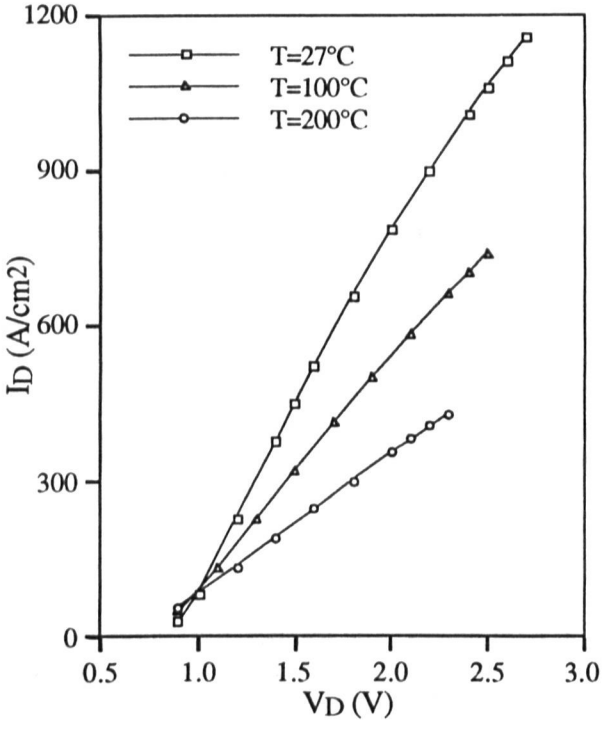

Fig.3. I_D-V_D characteristics at different temperatures (V_G=15V)

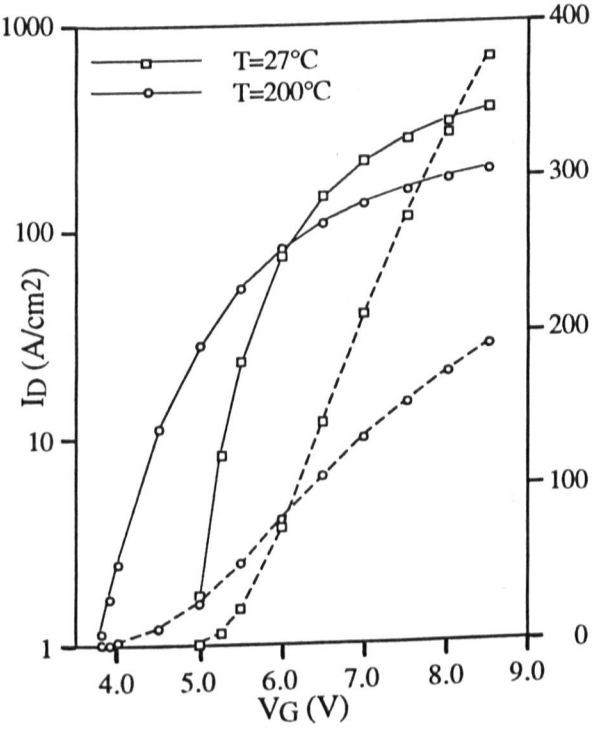

Fig.4. I_D-V_G characteristics at different temperatures (V_D=2V)

The high temperature has two main effects on the IGBT characteristics. Firstly the on-state current is reduced by over 50% as the temperature increases to 200°C as can be seen clearly from the I_D-V_D plot and also from the I_D-V_D plot for voltages above the threshold voltage. This means a significant increase in the on-state resistance and on-state power losses. The overall current decrease at 200°C is mainly due to the mobility reduction that decreases the MOSFET current and at the same time increases the resistance of the drift region. The larger voltage drop across the drift region at 200°C, as a result of higher resistance, is clearly seen in Fig.6(a). As can be seen from the comparison of the electron concentrations in Fig.5(b) and Fig.6(b) the carrier concentrations in the drift region in conductivity modulation mode are almost the same (approximately 10^{16} cm^{-3}).

The I_D-V_G characteristic reflects the MOSFET action of the IGBT gate and as such exhibits the kind of temperature dependence that is expected for a MOSFET [7,8,9]. This is a reduction in the current for voltages above the threshold associated with the drop in mobility, the lowering of the threshold voltage, and a decrease in the sub-threshold slope.

The second important effect at elevated temperature is the decrease in the static latch-up current associated with the turn on of the parasitic thyristor, which exists in the device structure [10]. In

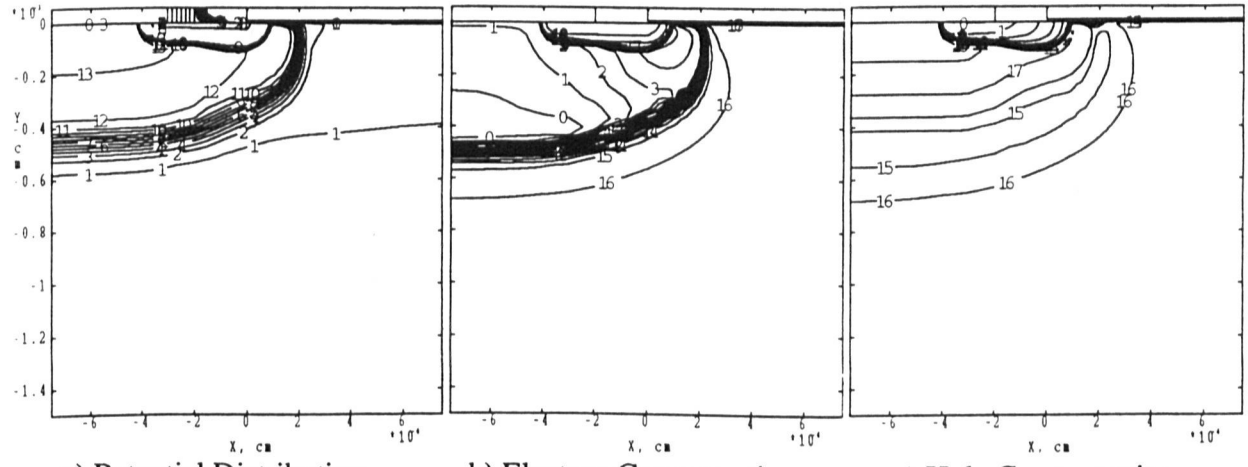

Fig. 5 Potential and carrier concentration distributions at room temperature (V_G=15V, V_D=2V)

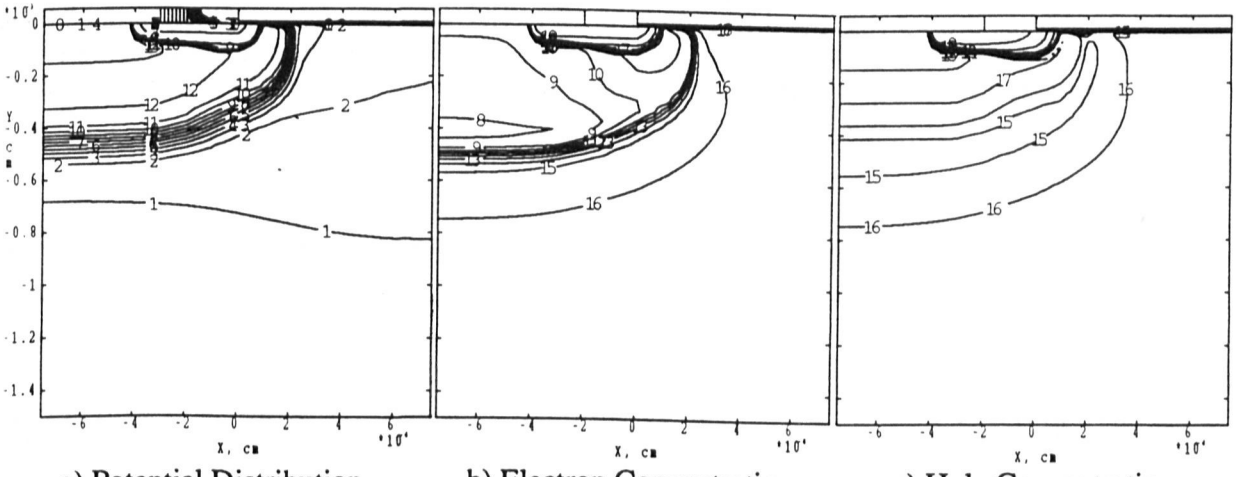

Fig. 6 Potential and carrier concentration distributions at 200°C (V_G=15V, V_D=2V)

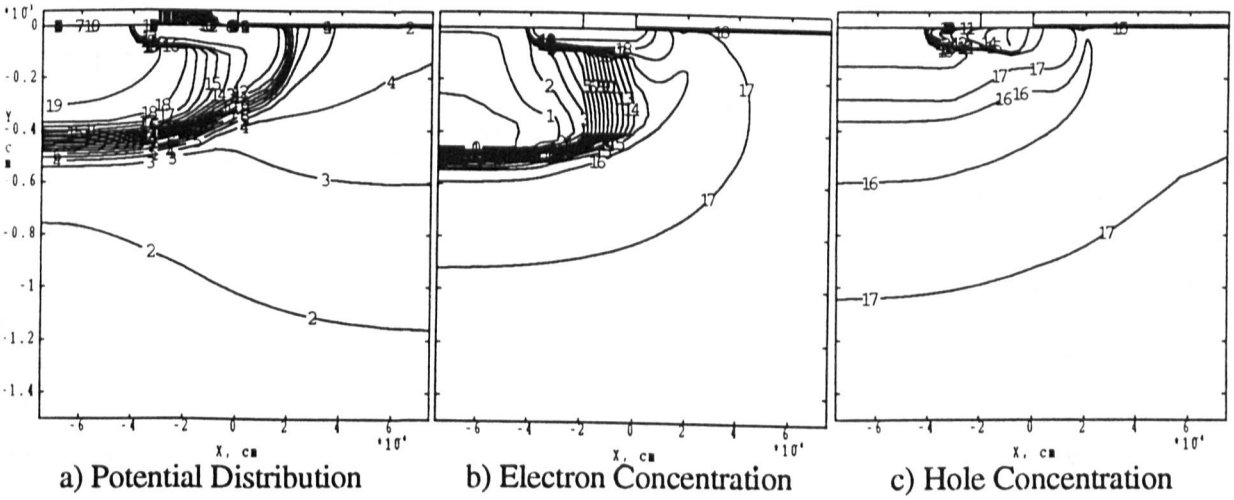

Fig. 7 Potential and carrier concentration distributions at latch-up (V_G=15V, V_D=3V, T=27°C)

the p-region the hole current flows around the n^+-region and due to the resistance of the p-region a voltage drop is produced. If the current is large enough then this potential difference will be sufficient to forward bias the n^+-p junction at the channel end injecting electrons from the n^+-region into the p-region, turning on the parasitic thyristor and latching up the device. At V_G=15V the static latch-up occurs at a current density of approximately I_D=1150A/cm^2 at room temperature and at I_D=440A/cm^2 at 200°C. The reduction in the static latch-up current is due to the reduction in the built-in potential of the n^+-p junction and to the increase in the resistance of the p-region. The potential, electron and hole distribution at latch-up are give in Fig.7(a,b,c). It is interesting to note that the latch-up occurs close to the channel, near the corner of the n^+-region.

IV. Conclusions

A program has been developed which is suitable for the simulation of IGBTs and which includes the temperature dependence of semiconductor parameters. The study of the high temperature IGBT's operation has shown that increasing the operating temperature of the device results in a significant reduction in on-state drain current for an applied drain voltage. The forward voltage drop across the drift region of the device also increases, as a result of increased resistivity, which leads to an increase in on-state losses. However this is accompanied by the lowering of the threshold voltage. The elevated temperature also reduces the maximum available drain current before latch-up of the device occurs.

Acknowledgements
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