# NUMERICAL SIMULATION OF ELECTROTHERMAL INTERACTIONS IN SEMICONDUCTOR DEVICES EXPERIENCING ESD PULSES

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## Abstract

The GIGA device simulator is used to simulate electrothermal interactions in devices with PN junctions under reverse ESD pulse conditions. GIGA provides a self-consistent time-domain solution of the heat flow equation, Poisson's equation, carrier continuity equations for electron and holes, and any associated circuit equations. Terminal currents and internal carrier concentration and lattice temperature profiles are calculated. The calculated temperature distribution permits identification of the location of "hot spots" that lead to device damage. GIGA is shown to be an effective engineering tool for designers of bipolar ESD protection devices.

## I. INTRODUCTION

Understanding the electrostatic discharge (ESD) destruction of devices with PN junctions, and optimizing ESD failure thresholds, are important aspects of designing IC protection circuits [1]. Self-heating of a semiconductor structure due to a high current pulse may cause electrothermal instabilities that lead to current filamentation and irreversible damage. Simulation gives physical insight into what mechanisms cause ESD destruction and how device designs can be altered to be more resistant to ESD.

Modeling ESD is difficult because time-dependency and lattice heating must be included when modeling electro-thermal interactions. Some work has been done in this area. 1D simulation of fully coupled thermal and electrical behavior of a diode structure was published in [2]. 2D simulation of electrothermal interactions within semiconductor devices under forward ESD pulse conditions was described in [3]. Simulation under reverse ESD pulse conditions was described in [4], but without accounting for the external circuit environment. The purpose of this study is to investigate thermal transient effects in semiconductor structures under reverse biased ESD pulse conditions taking into account interactions with an external circuit environment.

## II. ELECTROTHERMAL DEVICE SIMULATION

The GIGA device simulator [5,6] was used in this study. GIGA is a device simulator that self-consistently solves the drift-diffusion based semiconductor equations (Poisson's equation, and carrier continuity equations for electrons and holes), the heat equation in the semiconductor and in the heatsink, and electrical circuit equations.

GIGA models temperature dependencies and high level injection effects. The physical models incorporated into GIGA include: carrier mobilities that depend on doping, electric field, temperature, and electron and hole concentrations; temperature dependent effective band-gap narrowing; Shockley-Read-Hall (SRH) recombination, with doping and temperature dependent carrier capture times; Auger recombination; and temperature dependent impact ionization. The temperature dependencies of heat conductivities and capacitances of the cooling package are also included.

GIGA employs finite difference approximations. The coupled algorithm (Newton's method) is used for the electrical problem. The heat flow equation is solved self-consistently using a form of decoupled iteration. GIGA contains a one dimensional module and a two dimensional module. The one dimensional module is extremely fast, but can only be used up to the point where current filamentation starts [7]. The two-dimensional module permits very general investigation of thermal instabilities but is considerably more CPU intensive.

## III. RESULTS

The ESD destruction voltage of a $n^+$-p-$p^+$ diode structure was simulated first using the 1D module. The results were compared with experimental results obtained using the CV method [8]. The simulated structure was a 10 micron thick $n^+$-p-$p^+$ diode with a base concentration of 2E17 $cm^{-3}$ and peak surface concentrations of 1E20 $cm^{-3}$. The junction depth was 1.2 μm and the junction area was 500 $\mu m^2$. The external circuit consisted of 100 Ohms resistance and an initially charged capacitor. The previously validated failure criterion of dR/dT becoming negative within the structure was chosen [7]. Then for each arbitrary capacitance value of 100 pF, 200 pF, 500 pF and 1000 pF the initial capacitor voltage Vc0, applied to the structure in the reverse direction, was increased until the criterion for destruction was satisfied.

The calculated values of destruction voltage were close to the results presented in Figure 4 of [8]. Examination of the solutions for the 500 pF case indicates that the intrinsic temperature has been reached, and that within much of the structure the intrinsic carrier concentration exceeds the doping concentration in the p-base. The electron concentration is less than the doping concentration throughout the transients. In the calculations with 500 pF the negative dR/dT appeared at Vc0 = 190 V . The temperature (and intrinsic carrier concentration) distributions in this case had only one maximum and the shape of the corresponding curves did not change qualitatively over time.

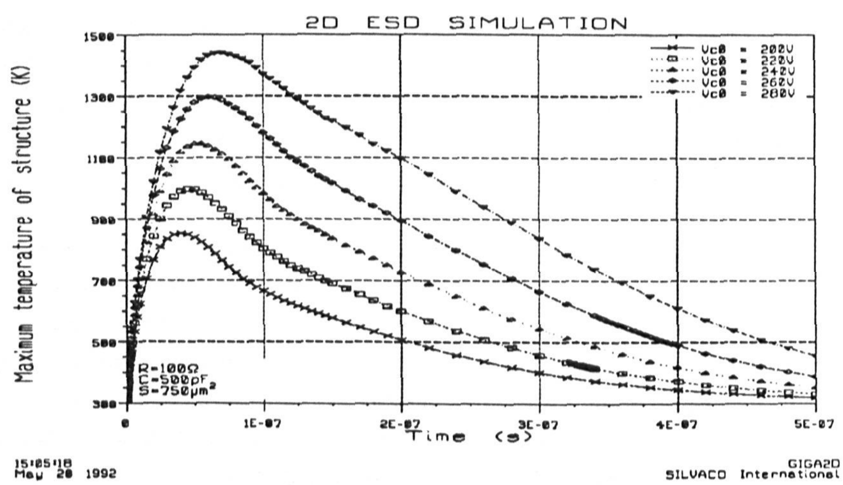


Figure 1. Maximum Temperature Versus Time

From examining the 1D and 2D results for S=750 $\mu m^2$ it was observed that the maximum temperature in 2D case (1000 K) exceeds the maximum temperature in the 1D case (700 K) by about 300 K.

Detailed 2D simulation were performed for the 100 Ohm and 500 pF case. The maximum temperature in the structure as a function of time for different values of reverse voltage is shown on Fig.1. The temperature reaches its maximum at t = 50 ns. The 2D temperature profile at the time instant t = 50 ns for Vc0 = 240 V is shown in Fig.2. A hot spot has appeared near the left emitter edge (at approximately at Y = 5 µm ). The temperature distributions in different horizontal sections at t = 50 ns indicate that there is a temperature maximum in the horizontal line at X = 1.5 µm. The temperature becomes much more uniform in the bulk (sections for X = 4.5 and X = 8.8 µm). The temperature dynamics along the vertical line Y = 5 µm is shown in Fig.3. After reaching its maximum at 50 ns temperature redistribution occurs, and the temperature maximum shifts into the bulk at t = 200 ns. Examination of the electron concentration dynamics indicates that along the vertical line Y=5µm (not shown) significant electron injection is caused by strong impact ionization in the pn junction region. The electric field magnitude along vertical line Y = 5 µm is shown in Fig.4. This shows that for time instants prior to 100 ns the electric field "fills" the entire p-base.This is due to significant hole injection caused by strong impact ionization. Thus injection compensates negative p-base doping charge and so the p-base behaves like an i-base. The filling of the entire base area means that voltage on the diode is significantly greater than static breakdown voltage.

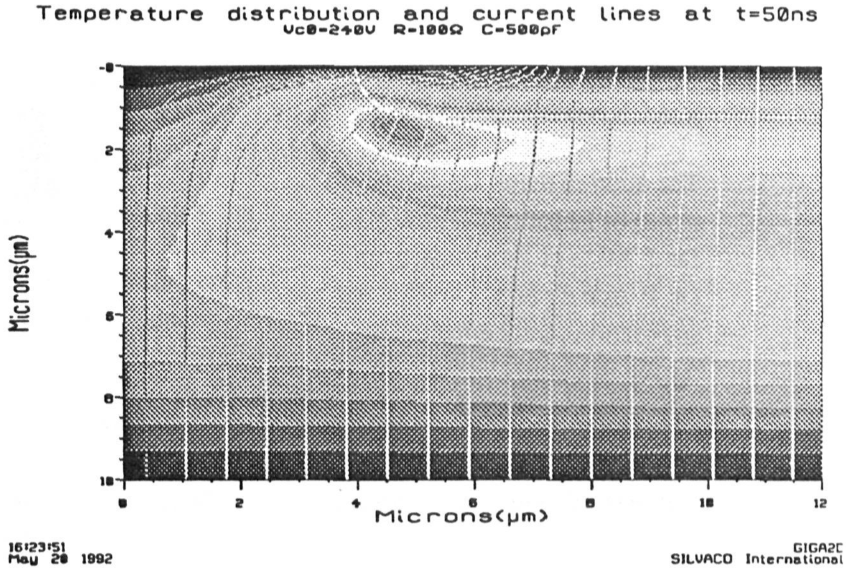


Figure 2. Current Flow Lines and Isotherms

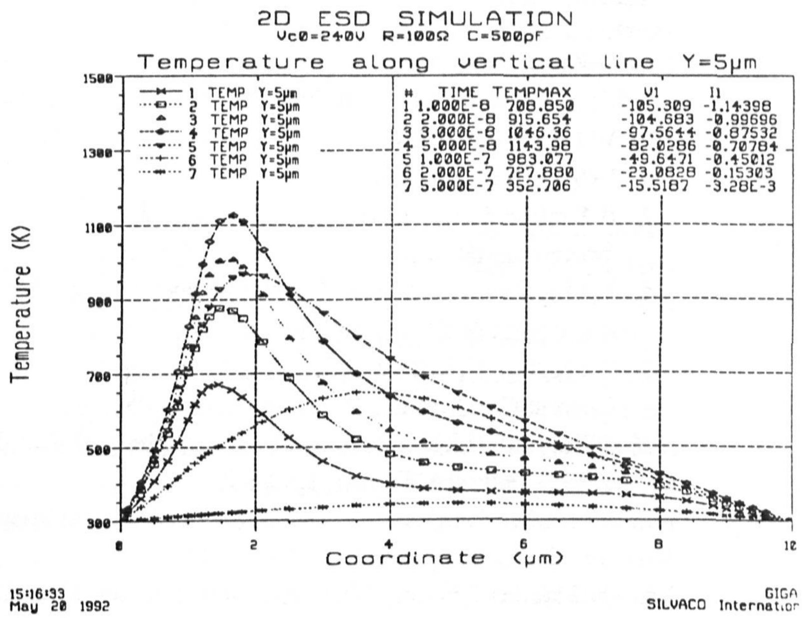


Figure 3. Temperature Distribution Dynamics Along Vertical Line at y = 5µm

## IV. CONCLUSIONS

The one-dimensional module of GIGA gives results that are in good qualitative agreement with ESD experiments. More detailed investigation accounting for more realistic 2D geometries can be performed using GIGA 2D. The two dimensional version of GIGA can predict the location of "hot" spots in structures. These results indicate that GIGA is an effective engineering tool for designers of bipolar ESD protection devices.

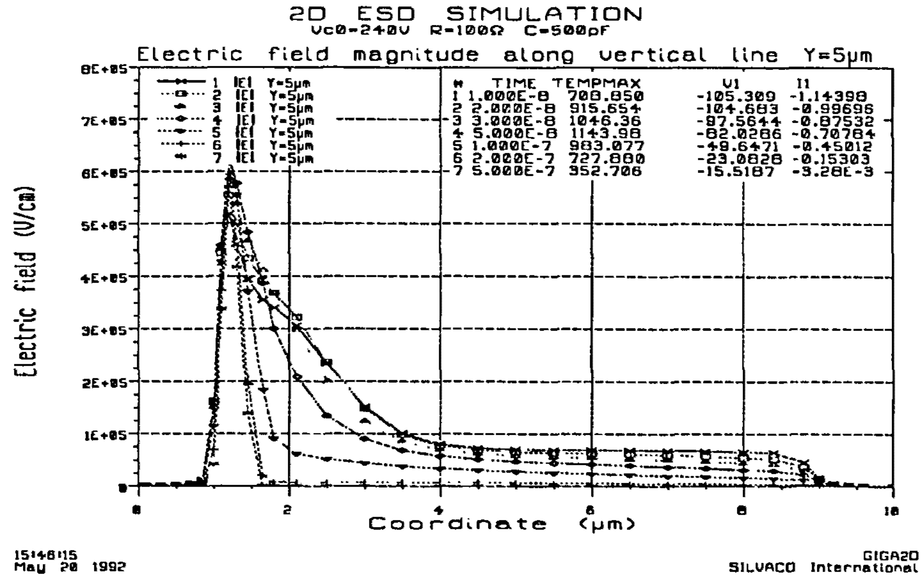


Figure 4. Electric Field Dynamics Along Vertical Line at y = 5 μm


## V. ACKNOWLEDGMENTS

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## REFERENCES


1. G.Krieger, "Thermal response of integrated circuit input devices to an electrostatic energy pulse", IEEE Trans. on Electron Dev., v.ED-34, N4, pp.877-882, 1987.
2. W.J. Orvis et al.,"Modeling and Testing for Second Breakdown Phenomena", in Proc. EOS/ESD Symp.,1983, pp. 108-117.
3. B.Krabbenburg, R.Beltman, P.Wolbert, A.Mouthan, "Physics of electro-thermal effects in ESD protection devices", in Proc.13th EOS/ESD Symp.,1991, pp. 98-103.
4. K.Mayaram, J.H.Chern, L.Arledge and P.Yang, "Electrothermal simulation tools for analysis and design of ESD protection devices", in IEDM Tech. Dig., 1991, pp.909-912.
5. B.Freydin, E.Velmre, A.Udal, "Failure Prediction of Power Devices under Reverse Surge Current Conditions", Proceedings of ISPSD'92.
6. B.Freydin, E.Velmre, A.Udal, "Electrothermal Simulation of Power Semiconductor Devices", 1991 VPAD Technical Digest, pp. 28-29.
7. A.L.Ward,"An electrothermal model of second breakdown", IEEE Trans. on Nuclear Science, vol. NS-23, N6, pp.1679-1684,1976.
8. N.Maeda, T.Wada, "The dependence of electrostatic destruction voltage on device structures of p-n junctions and insulated films", in Proc.11th EOS/ESD Symp.,1989, pp. 157-161.