Extraction of Charge Partitioning in Multi-Terminal Devices with AC Analysis Approach

*Ke-Chih Wu, Lydia So, Zhiping Yu, Robert W. Dutton, and John Faricelli**

Integrated Circuits Laboratory
AEL 231F, Stanford University, Stanford, CA94305, USA
*Digital Equipment Corp. Hudson, MA
Telephone: (415)725-3644 FAX: (415)725-7298

ABSTRACT

Low frequency, small-signal *ac* analysis of multi-terminal devices holds the promise of providing accurate charge partitioning information, which is of major concern to circuit designers. However, simple interpretation of the imaginary part of y–parameters as purely capacitive often leads to unphysical results when there are significant DC terminal currents. Although these 'abnormal' results in MOSFETs can be explained by the current sources in the equivalent circuit, extraction of charge partitioning from the conventional *ac* analysis is made impossible. A novel scheme is proposed using modified Jacobian in *ac* simulation for this purpose. Implementation of this scheme in PISCES leads to the results which eliminate negative capacitances while giving physically sound charge-partitioning information.

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The extraction of capacitance matrix is one of major tasks in MOSFET modeling for accurate circuit simulation. Various charge partition schemes [1], [2], [3] have been proposed for this purpose. Low frequency, small-signal *ac* analysis using device simulators such as PISCES and MINIMOS holds a great promise for this task since there is no need to make approximation which is inevitable for the analytical analysis. However, the simulation results using standard procedures [4] yield seemingly abnormal results at certain bias condition in so far as capacitance values are concerned. For bipolar devices, the reasons for such behavior have been well documented [5]. This paper presents an analysis of the abnormal results in MOSFETs and proposes a Jacobi-modification scheme which, when used with the standard procedure, provides a much better estimation of the charge partitioning, which is the basis for capacitance extraction.

These abnormal results manifest themselves in capacitances calculated for an electrode with significant DC current. For a MOSFET, this means that all the capacitances evaluated at either gate or substrate (C_{g*} and C_{b*} where * represents the excitation node) are correct while others (C_{s*} and C_{d*}) may have problems when the device is deeply turned on. The first column in Table 1 shows the results from a source excitation for a submicron MOSFET biased at V_{gs} = 4V, V_{ds} = 3V, and V_{bs} = 0V. In the four capacitances shown, two of them (C_{ss} and C_{ds}) fit the rule and have problem in interpreting the results. Indeed, the self-capacitance C_{ss} is negative, suggesting an inductive behavior, and is not equal to the sum of remaining capacitances. On the other hand, the magnitude of C_{ds} is much too larger. To understand this phenomenon, a look at the algorithm used in the *ac* simulation helps. The system of equations for *ac* analysis can be written as follows [4]:

$$\begin{bmatrix} J & -D \\ D & J \end{bmatrix} \begin{bmatrix} X_R \\ X_I \end{bmatrix} = - \begin{bmatrix} F_R \\ 0 \end{bmatrix} \tag{1}$$

where D is a diagonal matrix with element values proportional to the frequency under simulation. At low frequency, the contribution of X_I to the first set of equations can be ignored and (1) can solved in two steps:

$$X_R = - J^{-1} F_R \tag{2}$$

and

$$X_I = - J^{-1} D X_R \tag{3}$$

We now discuss the physical implication of this two-step procedure. The first step essentially calculates the *dc* solution resulted from the perturbation. And this *dc* solution becomes source (driving force) for evaluating the imaginary part in Eq. (3). In a sense, the second step can be viewed as the calculation of how each electrode would behave in charging the overall incremental charge. From the above discussion, it is clear that step one cannot be the source of the problem since it merely supplies the charge distribution caused by the excitation. The fact the total capacitance exceeds the value that is physically possible clearly indicates that the equivalent circuit network represented by the matrix J is not all passive, i.e., there are some active circuit elements in the equivalent circuit. As an result, the input, i.e.

the incremental charge distribution, has been amplified (or "distorted") to produce larger capacitance values. In fact, it has been known for long time that [6] the equivalent circuit network of semiconductor devices do contain current sources in any non-equilibrium state and their strength is proportional to the current density. Therefore, the imaginary part of current from *ac* analysis cannot be used to obtain the charge partitioning information since it reflects the *overall* response of the device in the presence of these current sources.

A natural conclusion from above discussion is that to extract the charge partitioning information, a Jacobian that representing a passive network should be used in the *second* step of the *ac* analysis. We have implemented this idea in PISCES program by properly modifying Jacobian for the *second* step. The Jacobian for the first step is kept unchanged. Figure 1 shows the capacitance curves for the diode in [4] generated by *ac* simulation, quasi-steady analysis, and our new scheme. It clear shows that the result from the new scheme agree with that of quasi-steady analysis very well while the curve from *ac* analysis turns negative as the diffusion capacitance effect starts to dominate. A comparison of the input capacitance (C_{bb}) of a bipolar transistor is shown in Figure 2. Since I_b is small, so is the discrepancy between *ac* analysis and the new scheme, consistent with the result in [5]. The second column of Table 1 shows the results from the new scheme. For the capacitances at the electrodes which have no *dc* current (C_{gs} and C_{bs}), the agreement with *ac* analysis is perfect. The capacitance between source and drain, C_{ds}, is slightly positive, consistent with the result one expects from charging a RC network.

In summary, our approach provides a way of determining charge partitioning for multi-terminal devices without making any *ad hoc* assumption. It has been reported that[5] the quasi-steady analysis (or called stored-charge model in [5]) is well suited in prediction of cut-off frequency for high-performance bipolar transistors. The physical implication of this observation is that stored-charge model captures the essential element in determining the high frequency behavior of semiconductor devices. By providing charge partitioning information based on total stored-charge, our approach is likely to be very useful for designers to model capacitances which are valid even at high frequencies.

References

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	Capacitance from Source Excitation (F/um)	
	AC	New
Cgs	-1.538E-15	-1.538E-15
Css	-3.6235-15	2.402E-15
Cds	6.364E-15	3.385E-16
Cbs	-1.202E-15	-1.202E-15

Table 1
Comparison of Capacitance Extraction Results

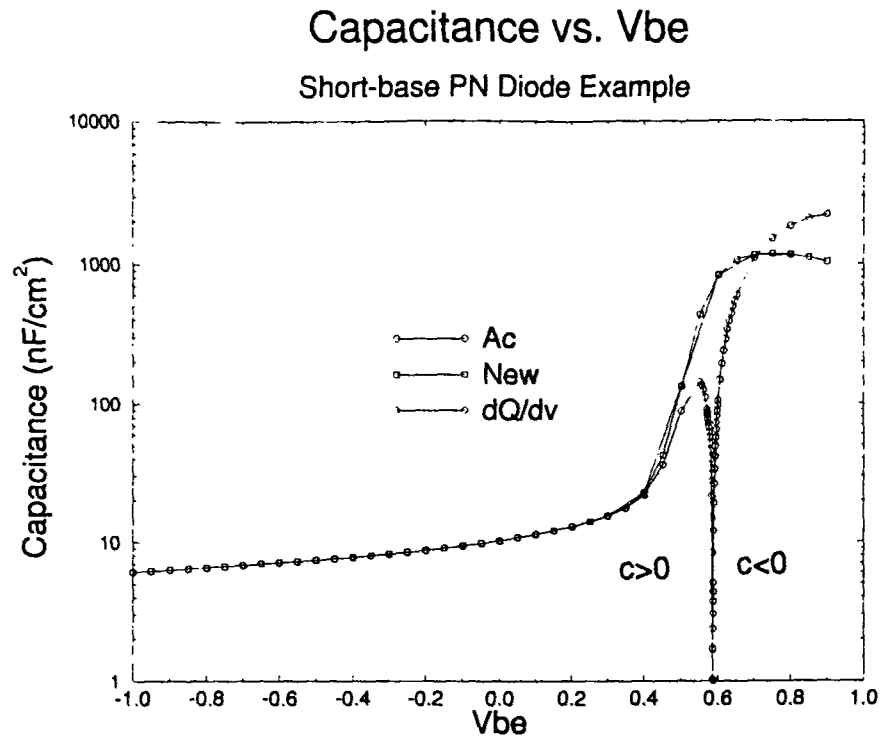

Figure 1
Capacitances of a short-base PN diode.

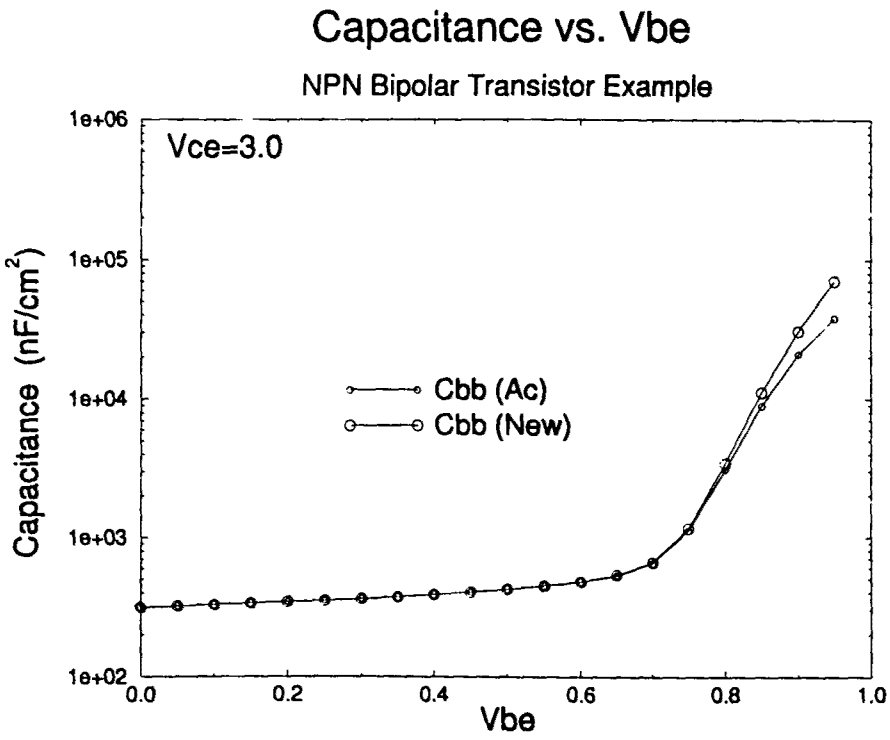

Figure 2
Input capacitances of a bipolar NPN transistor.