Multi-Subband Interface Roughness Scattering using 2D Finite Element Schödinger Equation for Monte Carlo Simulations of Multi-Gate Transistors

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Non-planar multi-gate transistors [1] are the preferred solutions for sub-16 nm digital CMOS technology thanks to superior electrostatic integrity and delivering a large ON-current. In this scaled process, interface roughness scattering (IRS) is considered to be a crucial factor for carrier transport [2], [3].

In this work, we have developed a new multi-subband IRS model which uses wavefunctions and energy levels from our 3D finite element (FE) Monte Carlo (MC) toolbox [4] with 2D FE Schrödinger equation quantum corrections [5]. The wavefunctions and energy levels are used to calculate a form factor entering the multi-subband scattering rate. The new multi-subband IRS model within 3D FE MC is then applied to 10.7 nm gate length SOI FinFETs with rectangular-like and triangular-like (Fig. 1) cross-sections describing their 3D geometry by the FE method and compared with a 3D Ando model.

A new multi-subband IRS model is incorporated into a 3D Finite Element Monte Carlo simulator using 2D Schrödinger equation based quantum corrections. The new 3D code is then used to forecast the performance of 10.7 nm gate length SOI Si FinFETs with two cross-sections: rectangular-like (REC) and triangular-like (TRI). We found that multi-subband IRS is much stronger at large electron kinetic energy resulting in reduction in the drive current to 600 mA/μm^2 for the REC shaped channel and to 498 mA/μm^2 for the TRI channel when compared to the results using the 3D Ando model. The multi-subband EPN model is based on a 2D formulation of Prange & Nee scattering model for arbitrary paths [6]. Wavefunctions at each eigenstate are extracted along the interface for all the slices (21 in our case) and unfolded onto an equidistant grid to calculate form factors as:

$$f_{n,n'}(s) = \psi^*_{n,k}\psi_{n',k'}\Delta V \qquad (1)$$

where n, n' are the initial and final energy levels, respectively, ΔV is the potential barrier between Si channel and high-κ dielectric. The IRS rate from the initial state n to the final state n' is:

$$\frac{1}{\tau_{n,n'}(E)} = \frac{1}{2\hbar}\int\limits_R |F_{n,n'}(q_\perp)|^2 C(q) dq_\perp g_{1D,n'}(E) \qquad (2)$$

where the $F_{n,n'}(q_\perp)$ is a fast Fourier transform (FFT) of the form factors, $C(q)$ is the exponential power spectrum and $g_{1D,n'}$ is the 1D density of states (DOS). The rate as function of initial energy is plotted in Fig. 2.

Figs. 3 and 4 show the I_D-V_G characteristics normalized by the area and Fig.5 illustrates average electron velocity along the channel of the TRI FinFET. The drive current, the drain induced barrier lowering (DIBL) and sub-threshold slope (SS) are collected in Table I. The average IRS rate monitored during the simulations as a function of initial electron energy at $V_D = 0.05$ V and 0.7 V (V_G-V_T = 0.7 V) is in Figs. 6 and 7. Fig. 8 shows electron density in the middle of the gate.

In summary, we have found that the multi-subband EPN IRS is stronger than the 3D Ando IRS at a large electron kinetic energy (from above 0.18 eV in the simulations of 10.7 nm gate length Si SOI FinFETs). The on-current is overestimated by the 3D Ando model by 36%, 44% for low and high drain biases, respectively.

References

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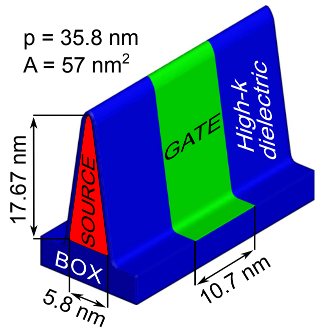

Fig. 1: Schematic of the simulated triangular-like shape Si SOI FinFET with a Gaussian doping profile where σ is 3.45 nm in the transport direction and has an effective oxide thickness (EOT) of 0.62 nm following the ITRS 2014.

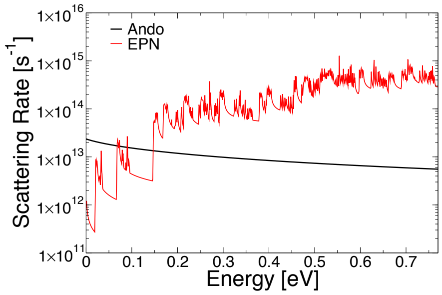

Fig. 2: IRS rate from 3D (Ando) and multi-subband Prange & Nee (EPN) models. The EPN is for the 20 lowest electron subbands of the device at $V_D = 0.05$ V and $V_G = 0.0$ V up to 0.77 eV but calculated up to 3 eV.

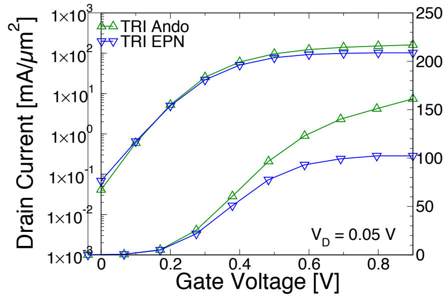

Fig. 3: I_D-V_G characteristics at $V_D = 0.05$ V using a normalised-to-area current for the 10.7 nm gate length TRI FinFET comparing the 3D interface roughness model (Ando) with the multi-subband model (EPN).

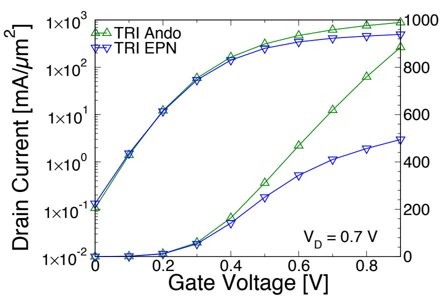

Fig. 4: I_D-V_G characteristics at $V_D = 0.7$ V using a normalised-to-area current for the TRI FinFET with a gate length of 10.7 nm comparing the 3D interface roughness model (Ando) with the multi-subband model (EPN).

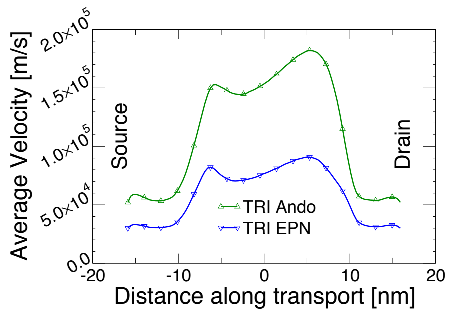

Fig. 5: Average velocity along the channel of the TRI FinFET at V_G-$V_T = 0.7$ V and $V_D = 0.7$ V.

Cross-section	TRI	
Lg [nm]	Ando	EPN
SS_{LOW} [mV/dec]	66	
SS_{HIGH} [mV/dec]	66	
$DIBL_{DD}$ [mV/V]	34	
$DIBL_{MC}$ [mV/V]	64	65
I_{MC}^{LOW} [mA/μm^2]	161	103
I_{MC}^{HIGH} [mA/μm^2]	885	498

TABLE I
SUB-THRESHOLD SLOPE (SS) AT $V_D = 0.05$ V AND 0.7 V FROM THE DD, DIBL FROM DD AND MC, AND DRIVE CURRENTS ($I_{MC}^{V_D}$) FOR THE TRI FINFET.

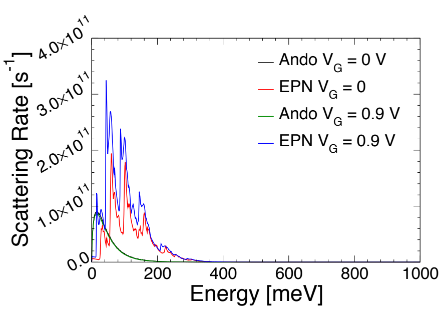

Fig. 6: Average scattering rate for TRI device at $V_D = 0.05$ V with 3D (Ando) and multi-subband (EPN) IRS models.

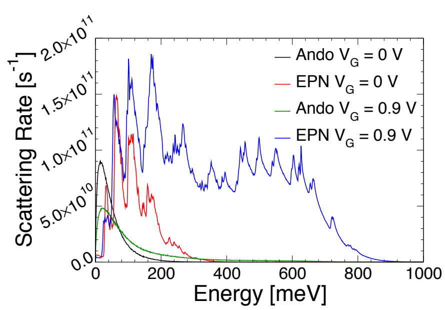

Fig. 7: Average scattering rate for TRI device at $V_D = 0.7$ V with 3D (Ando) and multi-subband (EPN) IRS models.

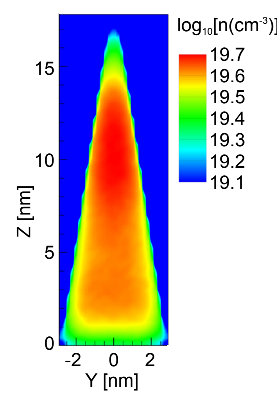

Fig. 8: Electron density in the middle of the gate in the TRI $\langle 100 \rangle$ FinFET at V_G-$V_T = 0.7$ V, $V_D = 0.7$ V using the new multi-subband IRS model.