A Rigorous Study of Nanoscaled Transistors Based on Single-Layer MoS_2

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Since the successful experimental isolation of graphene in 2004, ultra-thin two-dimensional structures are being widely studied as potential building blocks for future electronic devices. Among various two-dimensional materials, single-layer (SL) MoS_2 has attracted much attention. For a SL of MoS_2 a direct bandgap of 1.8 to 1.9 eV has been reported [1], which is suitable for various electronic applications. Recently, FETs based on SL MoS_2 with an $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio as high as $\sim 10^8$ and a sub-threshold swing of $\sim$ 70 mV/decade have been achieved [2]. However, the reported mobility is below that of ultra thin body or strained Si and III-V materials. It is believed that extrinsic sources such as charged impurities (CI) [3] and inevitable Schottky contacts [4] limit the characteristics of devices based on SL MoS_2. High-κ gate insulators, such as HfO_2, can reduce CI scattering effects and boost the mobility [3, 5], however, they can degrade the mobility due to remote phonon (RP) scattering [6] . The source of this scattering is in the surrounding dielectrics via long-range Coulomb interactions, provided that the dielectrics support polar vibrational modes.

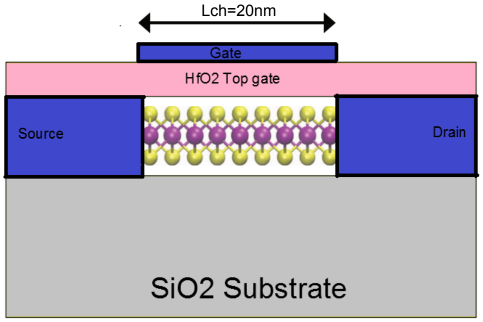

Fig. 1. Schematic view of the simulated device. An n-type top gate SL MoS_2 FET with ohmic contacts. The channel length is 20 nm and the gate oxide is 10 nm thick HfO_2 layer with $\kappa = 22$. The substrate is assumed to be SiO_2.

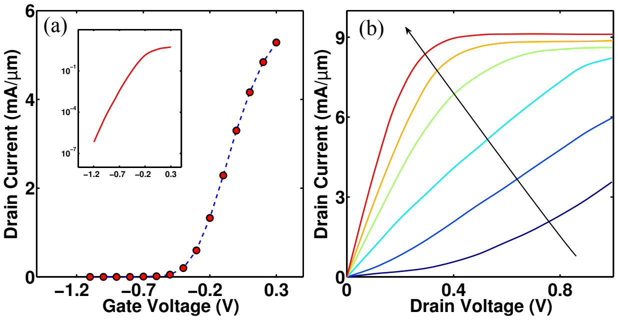

Fig. 2. (a) The transfer characteristics in the presence of scattering at V_{DS}=0.1 V. Transconductance is $g_m = 9.6$ mS/μ m. The inset shows transfer characteristics in logarithmic scale. (b) The output characteristics for V_{GS}= - 0.6 to +0.4 V with 0.2 V step (the arrow indicates the direction of V_{GS} increase). Current saturation is observed for $V_{\mathrm{DS}} > 0.3$ V.

To study electronic transport in SL MoS_2 we solved the NEGF equations self-consistently with the Poisson equation based on the box integration method. An effective mass of $m^* = 0.48m_0$ has been assumed for both longitudinal and transverse directions [7]. We have considered intrinsic electron-phonon interactions including the longitudinal acoustic (LA), the transverse acoustic (TA), the longitudinal optical (LO), and polar optical phonons (POP) with the parameters adopted from Ref. [7]. The mobility is calculated based on the method explained in Refs. [8, 9]. For device simulation we assumed a channel length of 20 nm, a 10 nm thick HfO_2 gate insulator, and a 50 nm thick SiO_2 substrate, see Fig. 1. In this study the dynamic screening of remote phonon modes stemmed from HfO_2 and static screening of charged impurities are included. Figure 2 shows the transfer and output characteristics in the presence of intrinsic phonon scattering. The results indicate a relatively high I_{on}

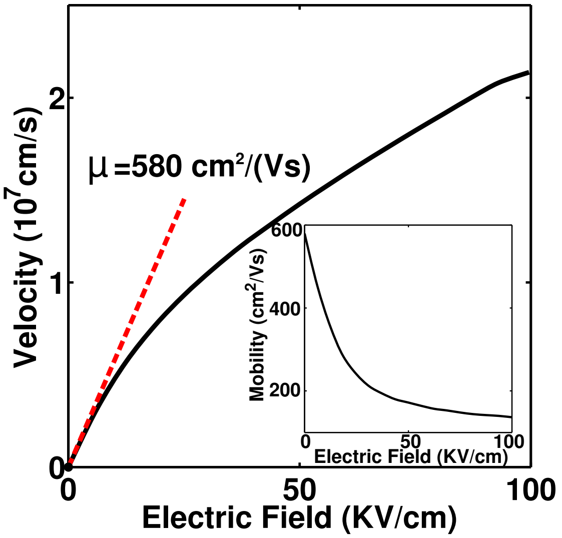

Fig. 3. The velocity as a function of the applied electric field. The inset shows the mobility as a function of the applied electric field. The low field mobility is about 580 cm^2/Vs and decreases to 130 cm^2/(Vs) under high electric fields.

of 9 mA/μm and a high $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio of about 10^7, which are close to the ballistic limit. Low field phonon-limited mobility is evaluated to be 580 cm^2/(Vs) in good agreement with the result of Ref. [7]. The effect of high fields on the mobility and carrier velocity are depicted in Fig. 3. The significant drop in the mobility is due to increased polar and non-polar optical phonon scattering at high electric fields.

Figure 4 shows the effect of CI scattering and RP scattering for an average carrier density of $\sim 10^{13}$ cm^{-2}. By using a high-κ insulator the CI scattering is suppressed which enhances the mobility. On the other hand, high-κ insulators introduce RP scattering which in turn reduce the mobility. Therefore, at low CI concentrations the mobility for a device with SiO_2 as the top gate is higher than that with HfO_2. Figure 4 shows the evaluated mobility in the presence of intrinsic phonons (IP), CI, and RP (CI+RP) is in good agreement with experimental results from Refs. [3, 10]. Table I compares the mean free path and the mobility for each scattering mechanism studied in this work. The results show that acoustic phonons play a more significant role in short channel devices than other intrinsic phonon modes. However, RP scattering due to a 30 nm high-κ HfO_2 results in the smallest mean free path. The presented results can be used for appropriate selection of the gate insulator material for optimal device performance.

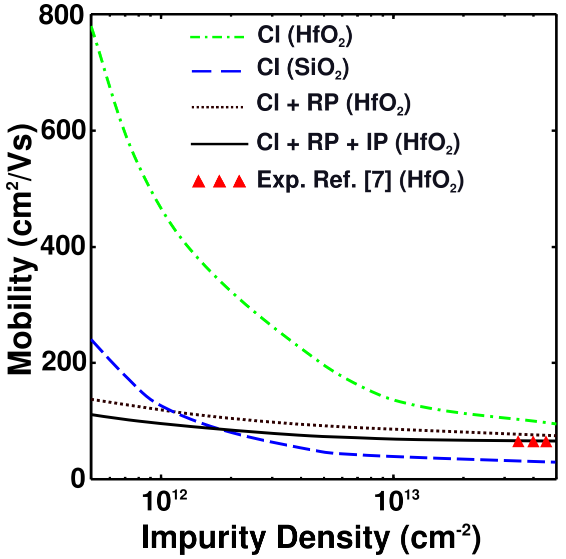

Fig. 4. Charged impurity (CI) and remote phonon (RP) limited mobility as a function of charged impurity density for 30nm thick HfO_2 and also SiO_2 top gate insulator. The mobility due to IPs+CI+RP with HfO_2 gate insulator is in good agreement with experimental results in Refs. [3, 10].

This work has been supported by the Austrian Science Fund (FWF), contract 25368-N30.

TABLE I

THE MEAN FREE PATH (λ) AND LOW-FIELD MOBILITY (μ) FOR EACH SCATTERING SOURCE. RP SCATTERING IS CALCULATED FOR FOR A 30 NM THICK HfO_2.

Phonon Modes	λ (nm)	μ (cm^2/(Vs))
LA+TA	35	923
LO	157	4161
POP	87	2316
RP	5.7	151

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