

Self-Consistent Physical Modeling of Silicon-Based Memristor Structures

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ABSTRACT

We employ a newly-developed three-dimensional (3D) physical simulator to study Si resistive switching nonvolatile memory (RRAM) structures. We couple a stochastic simulation of ion transport to the ‘atomistic’ simulator GARAND and a self-heating model to explore the switching processes in these devices. The model represents a significant improvement compared to the phenomenological models based on the resistor breaker network. The simulator is calibrated with experimental data, and reconstructs nicely the conductive filament (CF) formation and rupture in the 3D space.

INTRODUCTION

Nonvolatile memories based on resistive switching (memristors) offer improved controllability of charge in semiconductor memories at small sizes [1]-[3]. The development of memristor technology allows low cost-per-bit, low power dissipation, and high endurance. In addition, memristors can be integrated in crossbar arrays stacked in multiple levels in the 3D space [4]. The development of Si memristors, in particular, will result in a breakthrough in low-cost on-chip integration with Si microelectronics [1]. In this work, we present a self-consistent electrothermal simulation of intrinsic resistive switching in Si RRAM devices. Previous simulation work has relied on phenomenological models based on the resistor breaker network [5]. Furthermore, most work focuses on resistive switches based on metal oxides (e.g. HfO₂).

MODEL

We couple a kinetic Monte Carlo (KMC) simulation of ion transport to GARAND [6] and a time-dependent heat diffusion equation (HDE) solver to capture switching in the Si structure illustrated in Fig. 1, whose operation has been

demonstrated experimentally by our collaborators [1]. GARAND evaluates accurately the electric field and potential distributions by coupling the solution of Poisson's and density-gradient equations. Electrothermal coupling is achieved by solving the time-dependent HDE using the local Joule heating. In the simulation process, we update the traps' electron occupancies, by evaluating the hopping rates between the traps and the tunneling rates between the traps and the electrodes, which are used to calculate the steady-state current [2]. Fig. 2 illustrates the simulation procedure.

RESULTS, DISCUSSION AND CONCLUSION

A 3D volume under a poly-Si plate has been simulated, by considering an oxide thickness of 10nm and a simulation contact area of 40nm long and 20nm wide. Fig. 3 shows the I - V characteristics of the device, Fig. 4 shows typical temperature maps, and Fig. 5 shows the vacancy distributions up to the CF formation. At biases below 10V, few vacancies are created, giving very low currents. At around 10V, filament seeds appear and grow as bias is increased to 16V. At around 17V, an accelerated generation of oxygen vacancies occurs, forming a CF and bridging the p -Si substrate and the poly-Si terminal. The CF formation gives rise to an abrupt jump in the current, corresponding to the transition from the high resistance state (HRS) to the low resistance state (LRS). Temperature rise due to self-heating (up to 250K) plays a major role, as it affects the oxygen ion/vacancy generation probability and diffusion. A more detailed analysis will be presented to show the effect of self-heating, oxide thickness, and excess Si percentage on the device operation, including the electroforming, set and reset processes of the switching behavior.

ACKNOWLEDGMENT

We would like to thank the EPSRC (UK) for funding under the grant EP/K016776/1.

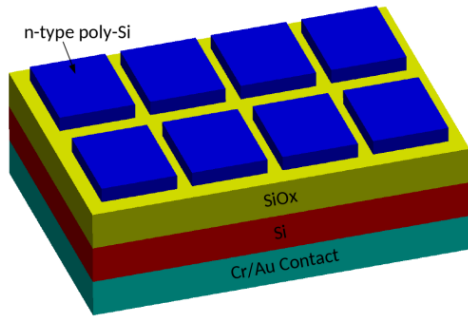


Fig. 1. The experimental memristor structure from Ref. [1].

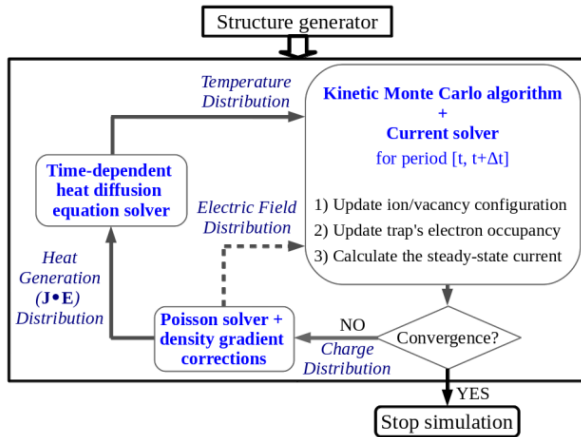


Fig. 2. The simulation framework.

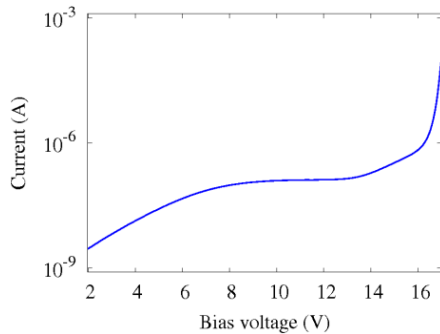


Fig. 3. The $I-V$ characteristics up to the CF formation. The currents are given for an equivalent width of 1mm.

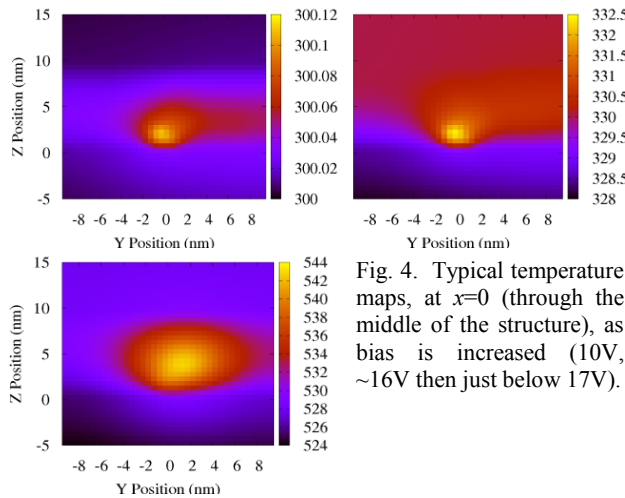
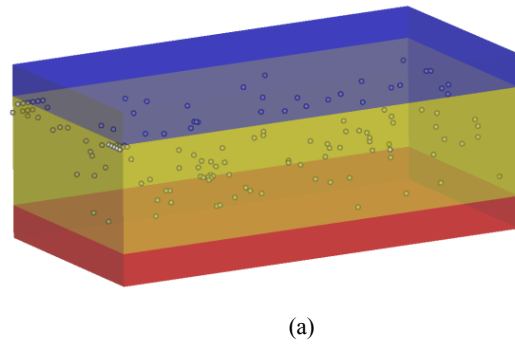
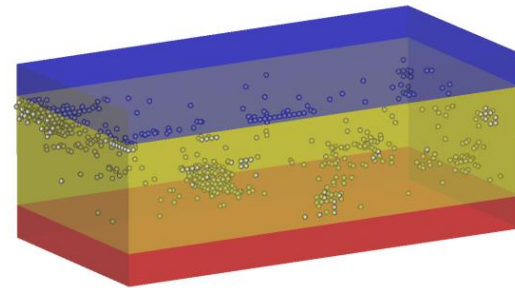


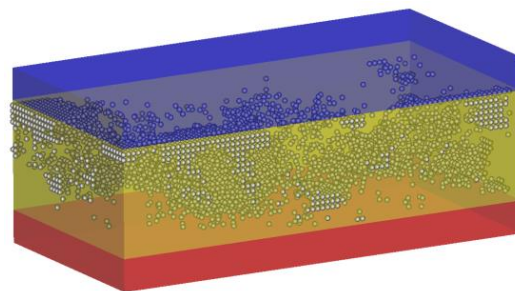
Fig. 4. Typical temperature maps, at $x=0$ (through the middle of the structure), as bias is increased (10V, ~16V then just below 17V).



(a)



(b)



(c)

Fig. 5. The vacancy distribution within the oxide, for (a) 10V, (b) 15V, and (c) 17V bias voltages.

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