Influence of quantum confinement effects over device performance in circular and elliptical silicon nanowire transistors

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INTRODUCTION

Silicon nanowire transistors (NWTs) are considered one of the most promising device architectures for the sub 7-nm CMOS technology [1]. In such ultra-scaled devices the quantum mechanical effects play a significant role that determines device performance [2]. These quantum confinement effects introduce a threshold voltage shift, simultaneously reducing the gate-to-charge capacitance and the charge in the channel available for transport [3]. Hence, in order to accurately describe the device performance in such ultra-scaled transistors, calculations that consider quantum mechanical effect are essential. In this paper, taking into account the quantum confinement effects, we establish a link between different cross-sections of two NWTs and the device performance.

METHODOLIGY AND DISSUSSION

Our simulations are based on a recently developed Poisson-Schrödinger (PS) quantum correction technology introduced in a drift-diffusion (DD) module of the GSS 'atomistic simulator' GARAND [4]. The 2D solutions of the Schrödinger equation are obtained in each cross-section along the gate length of the simulated transistor. The 2D Schrödinger equation is in an effective mass approximation [5]. The charge distribution obtained from the solutions of the 2D Schrödinger equation is used to define the effective quantum-corrected potential. This potential is used as a driving potential in the solution of the current-continuity equation, keeping the charge distribution in the NWT cross-section identical to the charge distribution obtained from the solution of the Schrödinger equation.

The nanowires simulated in this work have design parameters and geometry described in Tab. 1 and Fig. 1. The simulated NWTs have two cross-section shapes – cylindrical and elliptical (both have an identical cross-section area of 25 nm^2). The transport direction is aligned along the crystallographic orientation <110>.

Fig. 2 shows the capacitance-voltage characteristics (C-V) of both NWTs. From this data it is clear that the quantum mechanical (QM) effects have a significant impact on the gate capacitance. Overall, the QM gate capacitance is reduced by around 35% if compared to the classical DD simulations. This has a significant effect on the transistor's performance as the reduction of the gate capacitance reduces the mobile charge.

Fig. 3 presents the gate voltage dependence on the mobile charge in the channel for the discussed NTWs. A reduction of the gate capacitance, consistent with the results from Fig. 2, leads to a reduction of the mobile charge in the channel. Therefore a reduction in the NWT performance is also expected. Fig. 3 also shows a comparison of the 2D charge distribution in the NWTs cross-section based on the QM and classical DD simulations at V_G=0.6V. It is clear that the QM charge is predominantly localised in the middle of the channel while the DD solution shows increasing of the charge close to the semiconductor/insulator interface.

Fig. 4 shows the impact of the gate length on DIBL, defined as $\Delta V_T/\Delta V_D$, and on the sub-threshold slope (SS). As seen in Fig. 3, there is relatively little difference in the electrostatic integrity between the circular and elliptical NWTs. Hence, it can be concluded that the QM effects have no significant impact on DIBL and SS for these specific shapes of the cross-section for both NWTs.

The impact of the gate length on the leakage (I_{OFF}) and drive current (I_{ON}) is illustrated in Fig. 5. In this case there is a significant difference between the cylindrical and elliptical nanowire. Overall, the elliptical NWT shows lower I_{OFF} and higher I_{ON} current if compared to the cylindrical nanowire.

Fig. 6 reveals the 2D charges distribution and the first five wave functions with the lowest energy. It should be noted that for the circular nanowire the QM charge distribution inside of the channel is asymmetric, even though the wire has a symmetric cross-section. This is due to different effective masses in <110> crystal orientation along the two axes.

CONCLUSION

In conclusion, in this paper we report the effect of quantum mechanical effects on the electrostatic driven performance of NWTs suitable for the 7-nm CMOS technology. Overall, our work shows that the quantum effects cannot be neglected and that they determine the available mobile charge in the channel and gate capacitance.

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Si NTW	Circular	Elliptical
Diameter 1	5	4.16
Diameter 2	5	6
Oxide thickness	0.8 nm	
Channel Orientation	<110>	
Gate Length	6, 8, 10, 12, 14 nm	
V_D	50 mV and 700 mV	

Table I. Geometrical dimensions and the main characteristics for all silicon nanowires studied in this work.

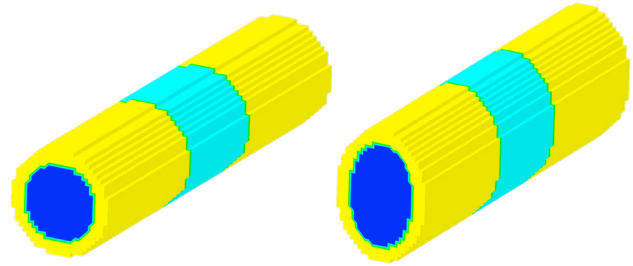

Fig. 1. 3D structure view of the circular (left) and elliptical (right) nanowire transistors. Dark blue is the Si channel, yellow is the SiO_2 oxideand light blue is the gate oxide.

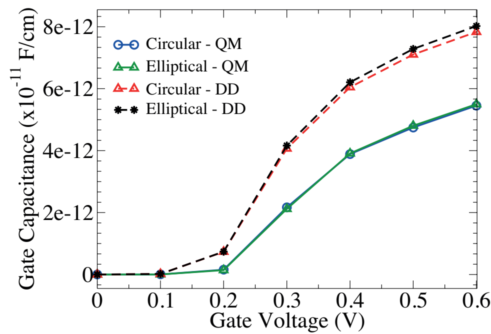

Fig. 2. Gate capacitance vs Gate voltage for the elliptical and cylindrical NWTs based on the classical (DD) and quantum mechanical (QM) calculations.

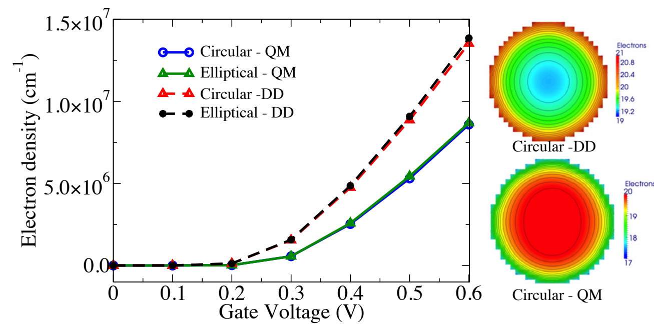

Fig. 3. Electron density vs Gate voltage for the elliptical and cylindrical NWTs based on the classical (DD) and quantum mechanical (QM) calculations (left); 2D charge distribution in the NWTs cross-section based on the QM and classical DD simulations at V_G=0.6V (right).

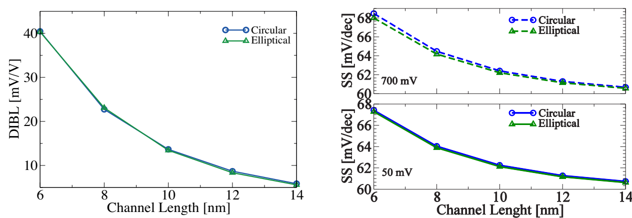

Fig. 4. Impact of the gate length on DIBL (left) and sub-threshold slope – SS (right) for the elliptical and circular nanowire with a 5x5 and 4.16x5 nm cross-section.

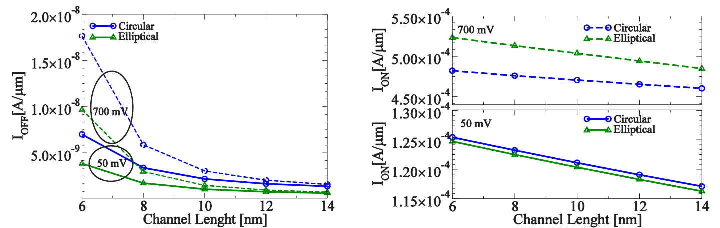

Fig. 5. Impact of the gate length on I_{OFF} (left) and I_{ON} (right) for the elliptical and circular nanowire with a 5x5 and 4.16x5 nm cross-section.

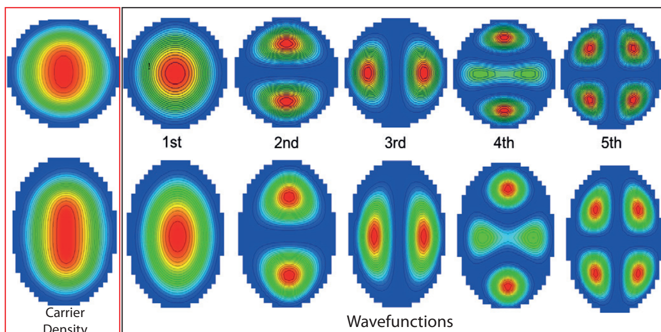

Fig. 6. 2D cross-sections (at the centre of the channel) of the simulated electron density and the first five lowest wave functions in the ON-state region.

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