Modeling of Parallel Electric Field Tunnel FETs

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ABSTRACT

Tunnel FETs with vertical tunnel paths are successfully modeled by the nonlocal band to band tunneling model. Although enhancement of ON currents are obtained by longer source gate overlap lengths, the increase of the ON current is not proportional to the lengths, because of non-uniformity of the band to band tunneling generations. It is explained by the peak generation rates at the source edge.

INTRODUCTION

Tunnel FET is a candidate for low power transistor alternative to CMOS. The authors have developed TFETs with vertical tunnel path called parallel electric field TFET (PE-TFET), and obtained enhancement of drive current by longer source-gate overlap lengths [1]. However the enhancement is less than proportional to the overlap lengths. The reason of this current degradation is investigated by device simulation with the nonlocal band to band tunneling (BTBT) model.

MODEL

Fig. 1 explains our scheme to obtain tunnel path lengths by tracing energy band profiles in the device simulator. The nonlocal electric field, defined as the band gap divided by the obtained tunnel path length is used to calculate carrier generation rate by famous Kane's formula. Accuracy of the model has been confirmed through comparisons to the experimental results of silicon TFETs [2]. Model parameters are not changed from conventional ones for silicon, and implemented into the device simulator [3].

PARALLEL FIELD TFETS

Fig. 2 shows the cross section of the PE- TFET. Assumed tunnel directions are shown by arrows in the figure. The drive current of the TFET is intentionally increased by tunnel areas increased by longer source-gate overlap lengths. The device is fabricated by epitaxial growth technique of additional silicon layer on the top of the source which is considered as the tunnel area.

SIMULATIONS

Device structures of the PP-TFET used in the simulation is schematically shown in Fig.3. The source concentration is 2×10^{20}cm^{-3}, effective oxide thickness is 1.3nm, the drain bias is -1V, and the epitaxial layer thickness T_{EPI} is 2nm. Fig.4 shows the comparison of measured and simulated on currents at V_{DS}=-1V, V_{GS}=-2.5V depending of the overlap length L_{OV}. It is successfully explained by the simulation that the on currents do not increase in proportional to L_{OV}. Fig.5 shows the simulated I_D-V_G characteristics in linear plot. It is clearly observed that the currents do not differ up to a certain gate voltage. This is because that the BTBT generation is mainly at the edge of the source junction, not covering whole the overlap region in these gate bias conditions. Fig.6 shows the BTBT generation rates at V_{DS}=-1V, V_{GS}=-2.5V, for the L_{OV}=200nm case. Even at this bias condition, the peak of BTBT generation rates is at the source edge, which is the reason that the ON currents do not increase in proportional to L_{OV}.

SUMMARY

TFETs with vertical tunnel paths are successfully modeled by the device simulation with the nonlocal BTBT tunneling model. The on currents do not increase in proportional to the source gate overlap length, because of the generation peak at the source edge.

ACKNOWLEDGMENT

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REFERENCES

[1] Y. Morita et al. "Performance evaluation of parallel electric field tunnel field-effect transistor by a distributed-element circuit model." *Solid-State Electronics* 102 (2014): 82-86.
[2] K. Fukuda et al. "On the nonlocal modeling of tunnel-FETs." SISPAD, 2012.
[3] HyENEXSS ver5.5.

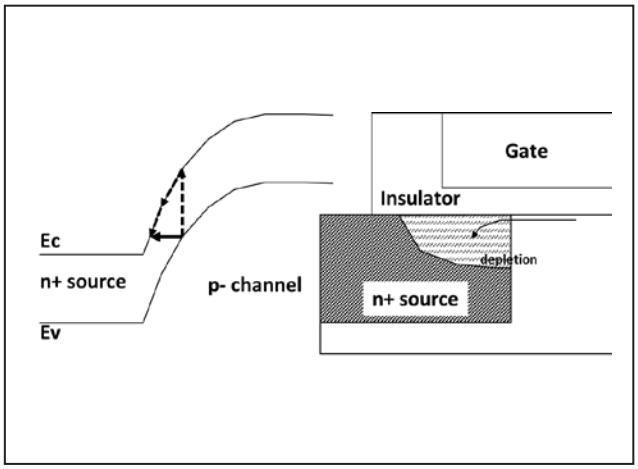

Fig. **1**. Trace algorithm of the nonlocal band to band tunnel model, band diagram (left) and 2D trace (right).

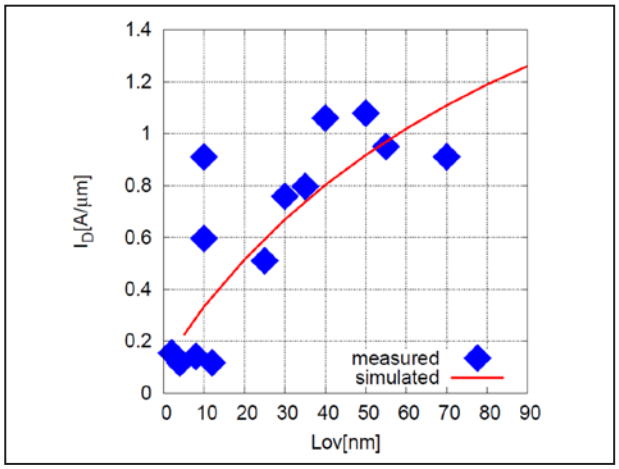

Fig. 4. Comparison of simulated and measured on-currents at V_{DS}=-1V, V_{GS}=-2.5V.

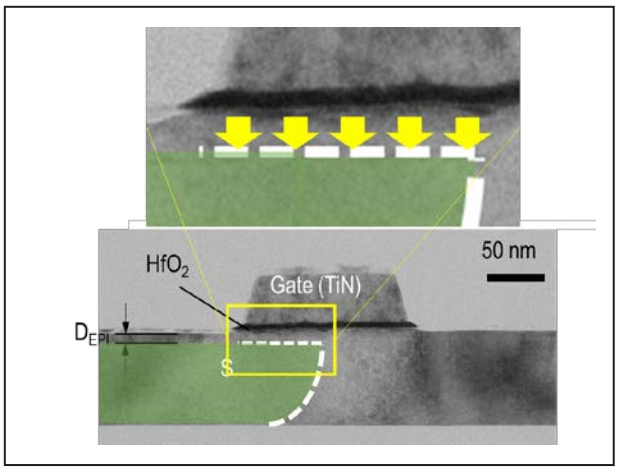

Fig. 2. TEM image of the PE-TFET and assumed tunnel directions.

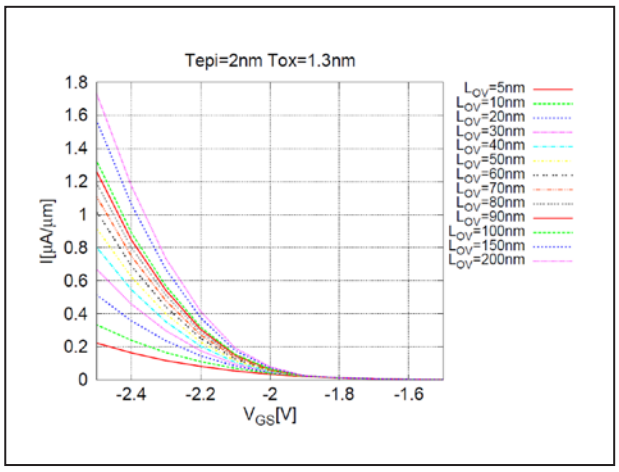

Fig. 5. The source and gate overlap length dependence of *I-V* curves simulated by the nonlocal BTBT model.

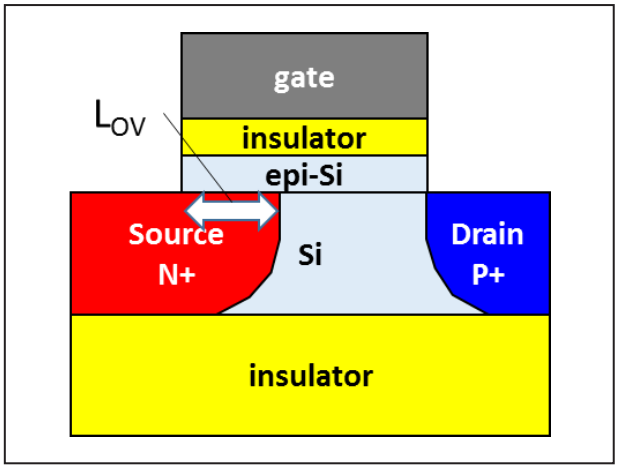

Fig. 3. Schematics of the PE-TFET simulated by device simulation.

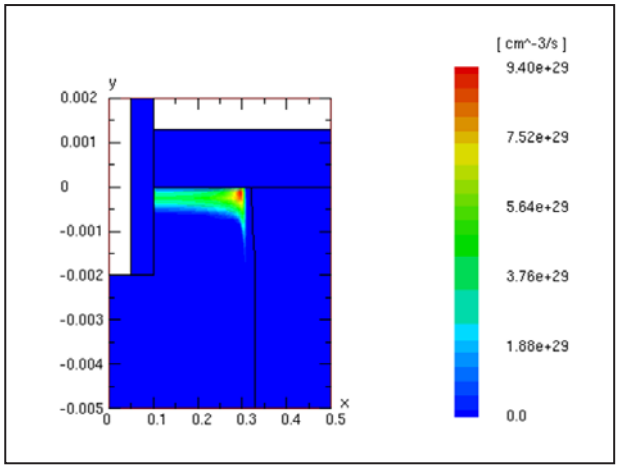

Fig. 6. 2D distribution of the BTBT generation rates for L_{OV}=200nm case.