Multi-Scale Modeling of Self-Heating Effects in Nano-Devices

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This paper discusses a multi-scale device modeling scheme for analyzing self-heating effects in nanoscale silicon devices. A 2D/3D particle-based device simulator is self-consistently coupled to an energy balance solver for the acoustic and optical phonon bath. This simulator is used to analyze the hot-spot temperature and location in various SOI devices, dual gate structures and nanowire transistors. This device simulator has been coupled to a SILVACO simulation tool which solves for heat transport in interconnects at the circuit level. The proposed multi-scale simulation scheme allows for analysis of thermal effects in an integrated circuit. Simulation results obtained with this simulator are in agreement with experimental measurements from IMEC using specialized heater-sensor test structures in common-source and common-drain configurations.

Since operating voltages do not scale proportionally to device size [1], scaling semiconductor devices towards the nanometer regime leads to a variety of unwanted phenomena. Among them, self-heating is of particular interest as it can degrade device performance. The mechanism for self-heating can be understood through the energy flow diagram in Fig. 1. Through the application of drain bias, electrons gain energy from the applied lateral electric field and interact with both optical and acoustic phonons. The majority of the electron energy is transferred to optical phonons. The zone center optical phonons practically have zero group velocity and the transfer of heat to acoustic phonons via anharmonic decay is very slow. This causes hot-spots to form. The elevated temperature in the active region of the device leads to enhanced phonon scattering, and therefore, mobility and current reduction. This effect is called self-heating [2].

Direct measurement of the temperature of the hot-spot is an impossible task; therefore, indirect methods have to be employed. One such method is the heater-sensor experimental structure (IMEC) [3]; the heater is the device under test (DUT) and the sensor determines the local temperature. This configuration uses the proximity of the heater to the sensor and the temperature dependence of the subthreshold slope of the sensor to infer the hot-spot temperature in the system.

To simulate the conditions in IMEC experiments, two significant changes were made to the existing simulator: (1) introduction of multiple terminals to model two transistors in common-source and common-drain configuration, and (2) coupling the thermal solver to a circuit level simulator to account for heat propagation in the interconnects. Important SILVACO modules that treat these self-heating effects are THERMAL3D and GIGA3D. This coupling, through a global Gummel loop is schematically illustrated in Fig. 3. In this arrangement, the SILVACO module simulates thermal transport characteristics at the interconnect level, providing temperature boundary conditions for the device-level simulation. The device level simulator then solves for the lattice temperature profile and the temperature of the hot-spot. The convergence of the global Gummel scheme is shown in Fig. 2. Joule heating power and inferred temperature of the hot spot are in agreement with experimental findings from IMEC.

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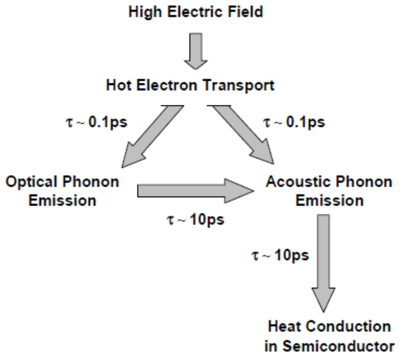

Fig. 1. This diagram shows the basic mechanism by which energy is exchanged between high energy electrons and the phonon bath.

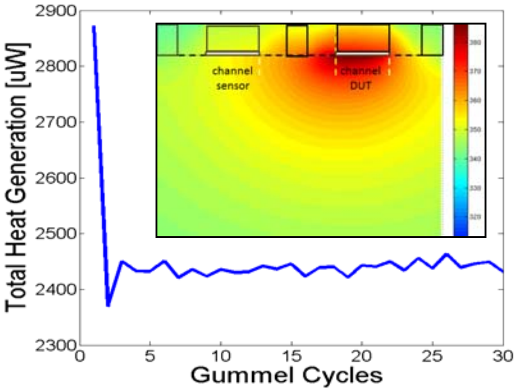

Fig. 2. Convergence of the global Gummel loop. Inset shows converged lattice temperature profile.

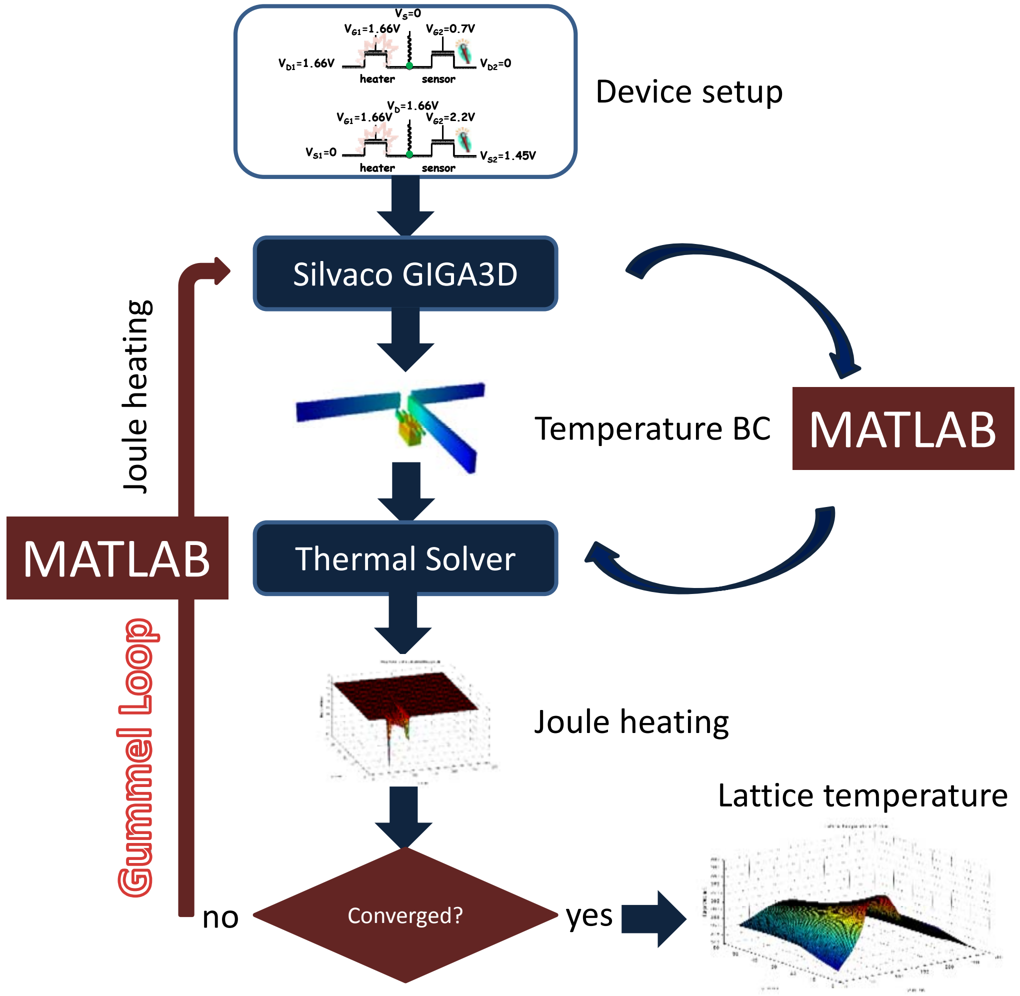

Fig. 3. Multiscale model implemented in this work.