Design Optimization of 14-nm Bulk FinFET Technology via Geometric Programming

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ABSTRACT

In this work, we for the first time optimize 14-nm Bulk FinFET design by using geometric programming (GP). By considering performance, design rule, and layout simultaneously, the problem is firstly modelled as a GP problem and an OPC's lithography simulation, a field simulation, and circuit simulation are performed for objective function evaluation.

1. INTRODUCTION

As the technology advances to 14-nm node and beyond, the number and complexity of design rules explosively grow up [1-2]. Early performance gains in early design rule development without cost increase and yield loss will benefit semiconductor industry [3-4]. In this work, the performance, the layout design, and the chip area co-optimization for design rule generation is modeled as a GP problem [5]. The device area is treated as an objective function and on-/off-state currents are considered as constraints. Advanced standard cell's GP is studied for 14-nm FinFETs. Main results show 30% delay improvement by this approach.

2. THE COMPUTATIONAL MODEL

We report a computational model to co-optimize the performance with electrical specification, the design rule with manufacturing constraint, and the layout design with technology process limitation. The co-optimization design is shown in Fig. 1. Statistical design of experiment (DOE) is used for each design rule, standard cell is designed based on process assumptions and then GDSII samples are auto-generated. To solve the large sample size problem, we implement a novel platform featuring systematic and statistical design rule evaluation to fast and accurately prioritize key design rules. As shown in Fig. 1, those selected samples are put into OPC's lithography [6] simulation and SPICE's circuit simulation. To search for the best sample, GP problem is applied. The objective function of the device's area is the product of a combination of vertical design rule and a combination of horizontal design rule. On-/off-state currents are considered as constrains [5].

Minimize **(before OPC)**

$$Area(R_1, R_2, ..., R_I, D_1, D_2, ..., D_J \mid M_1, M_2, ..., M_K) \quad (1)$$

s.t. **(after OPC)**

$$I_{on}(R_1, R_2, ..., R_I, D_1, D_2, ..., D_J \mid M_1, M_2, ..., M_K) \geq I_{on-set} \quad (2)$$

$$I_{off}(R_1, R_2, ..., R_I, D_1, D_2, ..., D_J \mid M_1, M_2, ..., M_K) \leq I_{off-set} \quad (3)$$

where R_1, R_2… and R_I are design rule values. D_1, D_2, … and D_J are design styles. M_1, M_2…and M_k are transistors. I_{on} and I_{off} are on-/off-state currents. $I_{on\text{-}set}$ and $I_{off\text{-}set}$ are targeted specifications. Set possible solutions of device's GP to be initial points for standard cell's GP problem:

$$T(R_1, R_2, ..., R_I, D_1, D_2, ..., D_J \mid C_1, C_2, ..., C_N) \leq T_{set} \quad (4)$$

$$P(R_1, R_2, ..., R_I, D_1, D_2, ..., D_J \mid C_1, C_2, ..., C_N) \leq P_{set} \quad (5)$$

where T is the delay time and P is the power. C_1, C_2, … and C_N are standard cells.

3. RESULTS AND DISCUSSION

To evaluate the design optimization via GP, design rules the "Contact2 Overlap Contact1" and the Ring Oscillator NAND2 with different bulk FinFET's widths are selected to generate GDSII samples. Delay distributions with 7 rings for those samples are simulated by field simulation for RC extraction and by circuit simulation for cell's electrical behaviour. Fig. 2(a) shows the ground rule (GR) value is manually set up based on the simulation data. However, 6 FINFET still suffers 2% performance degradation. Fig. 2(b) shows, after GP optimization, different FinFET's widths are automatically set with respect to different GR values. No performance degradation issues exist. Fig. 2(c) shows no performance degradation issues for 2 FINFET under different corners after GP optimization. Fig. 2(d) further shows the GP optimized performance for the "Poly Pitch" design.

4. CONCLUSIONS

In summary, design optimization of 14-nm bulk FinFET's via GP has shown performance degradation can be improved without increasing chip size and yield lost. Notably, all rules are optimized simultaneously.

5. ACKNOWLEDGEMENTS

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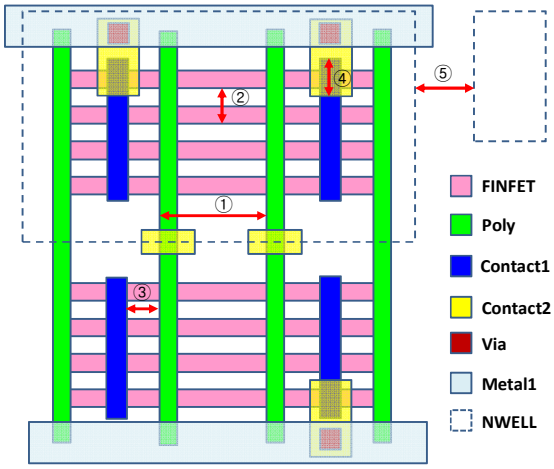
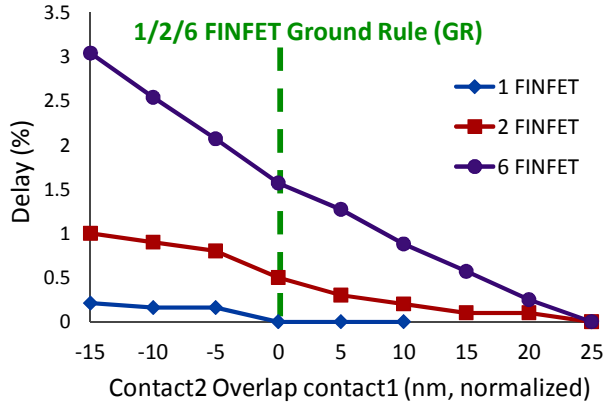


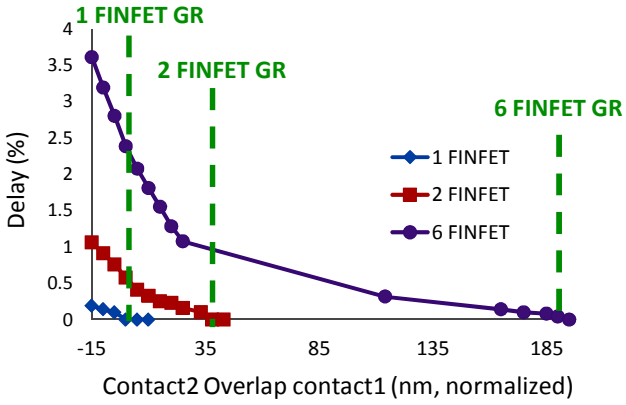
	Design Rule	Performance Concern	Yield Concern	Chip Area Concern	Design Rule Generation Method
①	Poly Pitch	I_{on}, I_{off}, V_t	Open, Short, Gate Height	Lateral	Lithography Simulation & Cost Reduction
②	FinFET Pitch	I_{on}, I_{off}, V_t	Open, Short, Fin Height	Longitudinal	Lithography Simulation & Cost Reduction
③	Contact1 to Poly Space	-	Contact1 to Poly Short	-	Lithography Simulation & Analytical Equation
④	Contact2 Overlap Contact1	Overlap Resistance	Overlap Alignment	-	Lithography Simulation & SPICE Simulation
⑤	NWELL to NWELL Space	Breakdown Voltage	-	Lateral	Electrical Characteristic Assessment

(a) (b)

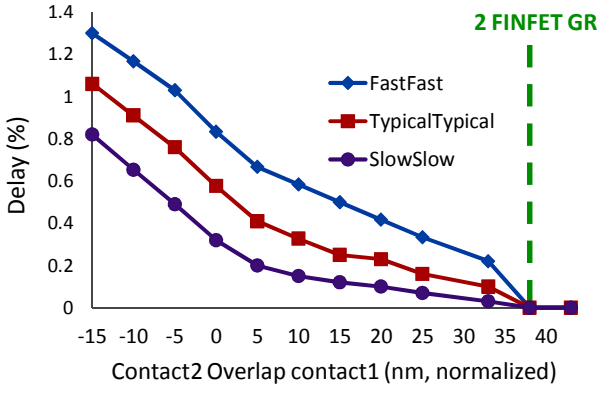
Fig. 1. (a) Pattern of the studied bulk FinFET NAND2 layout with key design rules. (b) List of performance concern, yield concern, and chip area concern for the key design rules of FINFET NAND2. The last column shows the design rule generation method for the key design rules of FINFET NAND2.



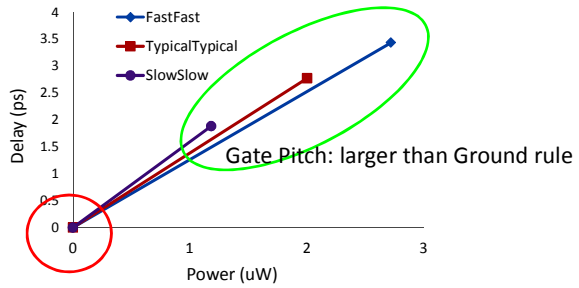
(a)



(b)



(c)



(d)

Fig. 2. NAND2 RC extraction and SPICE simulation. (a) Without GP optimization, GR of "Contact2 overlap Contact1" is set up to be the same for 1/2/6 FINFET. This result shows 6 FINFET has performance degradation issues around 2%. (b) With GP optimization, GR of "Contact2 overlap Contact1" is set up to be different for 1/2/6 FINFET. This result shows no performance degradation issues under typical corner. (c) With GP optimization, this result shows GR of "Contact2 overlap Contact1" has no performance degradation issues for 2 FINFET under different corners. (d) With GP optimization, GR of "Poly Pitch" has better performance in smaller value.