

# Effect of Impurity Scattering on Mobility in Si Nanowire Junctionless FETs

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## INTRODUCTION

Conventional inversion-mode MOSFET faces the limit of scaling down due to the short channel effect and the difficulty of the fabrication process. The junctionless transistor (JLT) is one of the alternative devices to overcome the problems[1]. In JLTs, the homogenous atoms are doped uniformly in the contact and channel regions. The current of the JLTs flows the center of the cross section of the nanowire since the current is turned on in the condition of the flat band. To obtain the sufficient on-state current, the heavy doping is required. Consequently, the effect of the impurity scattering on the transport properties is crucial in JLT. In this paper, we investigate the effect of the impurity scattering on the current and the mobility to the nanowire JLT with a small cross section where the quantum confinement is dominant.

## MODEL

The schematic picture of the n-type circular gate all around nanowire JLT is shown in Fig. 1. The all regions in Si nanowire have the doping concentration of  $4 \times 10^{20} \text{ cm}^{-3}$ . The discrete ionized dopants P are located in the center of the cross section inside the channel. The gate length  $L_c$  extends from 10.5 nm to 42nm. The radius of the cross section of the wire is 1.5nm.

The electronic structure of the nanowire is calculated with a  $sp^3d^5s^*$  tight binding model. The current is calculated by the nonequilibrium Green function (NEGF) method[2]. The electrostatic potential and electron concentration are determined by solving the NEGF method and the Poisson equation self-consistently.

The  $dR/dL$  method is adopted to derive the impurity-limited mobility[3]. The mobility is calculated as

$$\mu = [dR / dL_c]^{-1} \frac{1}{en_c}, \quad (1)$$

where  $n_c$  is the number of electrons per channel length.

## RESULTS

We calculate the current  $I_d$  as a function of the gate voltage with the different channel lengths ( $L_c = 10.25, 31.5, 42$  nm), respectively as shown in Fig. 2. The bias voltage is fixed to  $V_d=0.001\text{V}$ .  $dR/dL_c$  is determined by three data points for each  $V_g$  as shown in Fig.3. The mobility is calculated by Eq. (1) where  $n_c$  is derived from the lesser Green functions. In Figs. 4 and 5, the mobility is plotted as a function of the gate voltage and the number of electrons per channel length. The gate voltage increases the number of electrons inside the channel. The mobility significantly enhances with increase of electrons inside the channel region. This is due to the screening of the ionized impurity potential by carriers which becomes dominant when the carrier concentration is larger than  $10^{19} \text{ cm}^{-3}$ . This phenomenon is particular to JLT since the impurities have same polarity as the carriers have.

## CONCLUSION

We have examined the mobility in the presence of the ionized impurity scattering of the n-type nanowire junctionless FETs. We have found that the mobility has become larger with the increase of the density of the electrons inside the channel by tuning the gate voltage, which can be results from the screening of ionized impurity potential due to the transporting electrons. The results may provide the guide for devices with improved transport properties.

## REFERENCES

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- [3] M. Luisier, *Phonon-limited and effective low-field mobility in n- and p- type [100]-, [110]-, and [111]-oriented Si nanowire transistors*, Appl. Phys. Lett. vol. **98**, 032111 (2011).

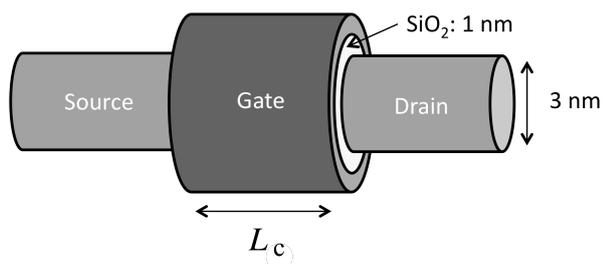


Fig. 1. Schematic picture of a Si gate-all around circular nanowire JLT.

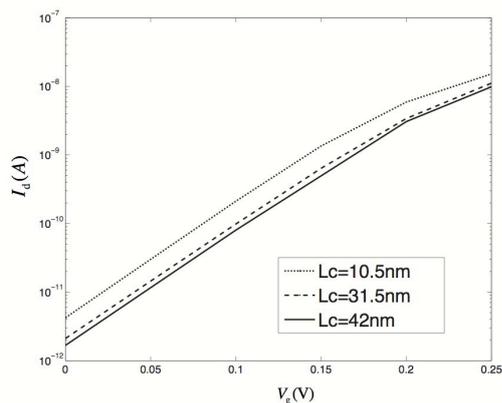


Fig. 2. Current  $I_d$  as a function of the gate voltage  $V_g$ .

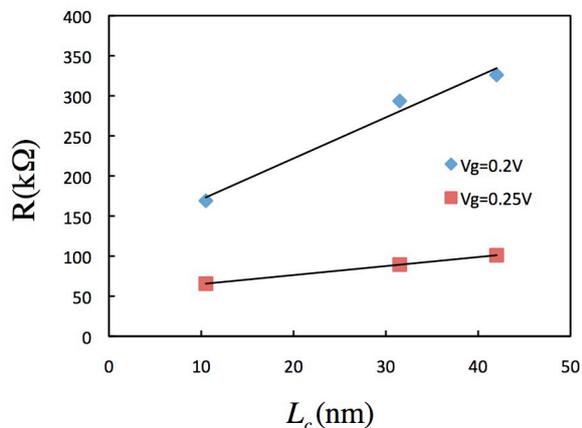


Fig. 3. Channel resistance  $R$  as a function of the channel length  $L_c$ .

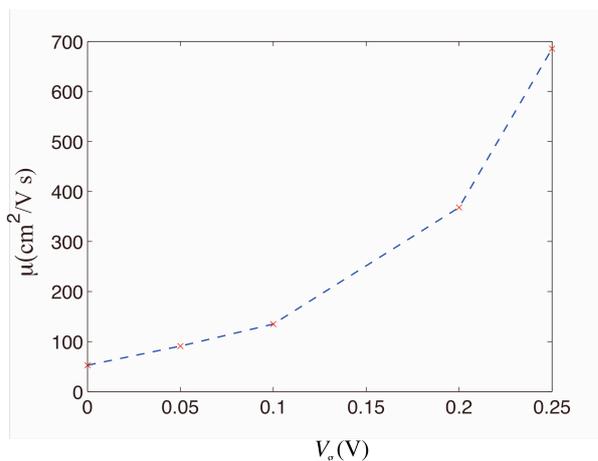


Fig. 4. Mobility  $\mu$  as a function of the gate voltage  $V_g$ .

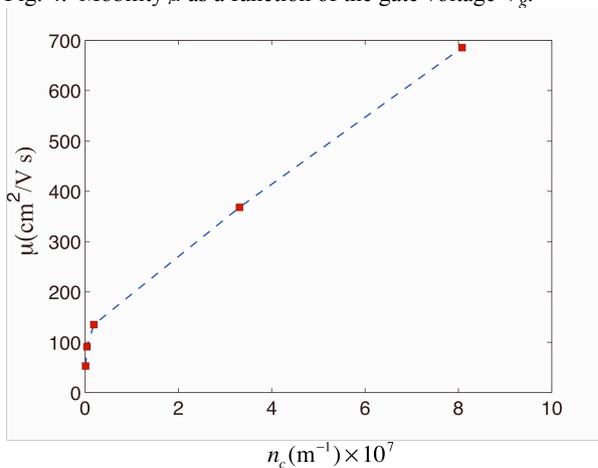


Fig. 5. Mobility  $\mu$  as a function of the number of the electron per channel length  $L_c$ .