TiN Work Function Variability on Ultra-scaled FinFETs using a NEGF formalism

 R. Valin, A. Garcia-Rivera^{*}, M. Aldegunde, A. Martinez, and J. R. Barker[§] College of Engineering, Swansea University, UK
*CITIUS, University of Santiago de Compostela, Spain
[§]School of Engineering, University of Glasgow, G12 9YH, UK e-mail: r.valinferreiro@swansea.ac.uk

Metal work function variability (WFV) is one of the largest sources of fluctuation in nanoscale Mosfets [1]. Semi-classical simulations of metal work function variability (WFV) have demonstrated that the threshold voltage variation increases as a function of the grain size. Reaching the maximum variation when the grain size is in same the order as the gate length [2]. This work presents a WFV study of Titanium Nitride (TiN) metal-gate granularity on an ultra-scale silicon 5.4nm channel length Trigate FinFET. The FinFET thickness is 4.2nm and the finheight is 10.6nm. The equivalent oxide thickness of the gate is 0.48nm. The channel region is undoped and the length of source and drain regions is 10nm. We deploy a Non-equilibrium Green's Function (NEGF) formalism to describe carrier transport as the channel length is under 10nm and a substantially amount of tunnelling is expected. To the best of our knowledge, this is the first study of WFV on FinFETs using a full quantum transport formalism. In order to simulate metal-gate granularity the Voronoi method has been implemented following the methodology explained in [2]. The diameter of the simulated TiN grain size is 5nm. Since the grain area $(pi \times (qraindiameter)^2/2)$ is in the order of top gate area there is only one grain in this region. To take into account the effect of neighbour gates, the gate geometry has been unfolded to calculate the Voronoi patterns. Table I shows the work function probability of the tow TiN orientations considered in the simulations [3]. The two possible work functions of the gate can be seen in Fig. 1 after mapping the Voronoi patterns to the physical gates of the FinFET. The matching between the Voronoi patterns and the gate potential is shown in Fig. 2. This figure shows three metal grains for the lateral gates and only one

for the top gate. Three regions are shown in the Voronoi pattern of the top gate, two of them due to the interaction with lateral gates (green areas) and the other one is created by the unique metal grain of the top gate. The WFV is affecting the control over the channel changing the barrier height such as is shown in Fig. 3. This figure represents a subset of the total simulated devices. The change of the barrier height depends on the size and location of the metal grains and the interaction with the neighbours. The effect of WFV on the drain currentvoltage characteristics at $V_D = 0.7V$ is shown in Fig. 4 where the mean of the curves is slightly shifted according the work-function probability. The drain current dispersion is quite large inducing a large threshold voltage variability. This variability follows a normal distribution as can be seen in Fig. 5 with a threshold voltage deviation equal to 42mV. Our results are consistent with those obtained in reference [2] when the ratio between grain size and gate length is approximately one. As a conclusion, these results demonstrate a large threshold voltage variability coming from metal grains for ultra-scaled FinFETs.

REFERENCES

- R Huang et al. Variability investigation of gate-allaround silicon nanowire transistors from top-down approach. In 2010 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), pages 1–4. IEEE, (2010).
- [2] Shao-Heng Chou et al. Investigation and Comparison of Work Function Variation for FinFET and UTB SOI Devices Using a Voronoi Approach. *IEEE Transactions on Electron Devices*, 60(4):1485–1489, (2013).
- [3] Hamed Dadgour et al. Modeling and analysis of grainorientation effects in emerging metal-gate devices and implications for SRAM reliability. In 2008 IEEE International Electron Devices Meeting, pages 1–4. IEEE, 2008.

TABLE I: Probability and work-functions of TiN metal grains.

Orientation	<200>	<111>
WF	4.6eV	4.4eV
Probability(%)	60	40



Fig. 3: First subband representation of different metal grains configurations at $V_D = 0.7V$ and $V_G = 0.3V$.



Fig. 1: Potential representation of the Trigate Fin-FET at $V_G = 0.1V$. The effect of TiN metal grains on the gate boundary conditions has been highlighted with blue and green colours.

ò

 $\chi_{(nm)}^{10}$

otential (V)

20



60

Fig. 4: Current dispersion of different metal grain configurations of Trigate FinFET at $V_D = 0.7V$. The mean of the current is highlited with a red line.



Fig. 2: Voronoi surfaces and corresponding potential of the lateral and top sides of the the TiN Trigate FinFET. The potential at $V_G = 0.1V$ for two different Voronoi patterns.



Fig. 5: Threshold voltage distribution of different metal grain configurations of Trigate FinFET at $V_D = 0.7$ V. $\sigma V_{th} = 42mV$.