Influence of device geometry on electrical characteristics of a 10.7 nm SOI-FinFET

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The scaling of MOSFET devices to nanometer dimensions leads to an increment in the short channel effects (SCE). To mitigate this problem new materials and architectures have to be studied. SOI-FinFETs are currently considered one of the most promising solutions to avoid SCEs.

Along with other sources of statistical variability affecting nanoscale transistors: line-edge roughness (LER), random dopants (RD) or the orientation of the grains that compose the metal gate (MGG) already studied in a 25 nm gate length SOI FinFET [1], the physical geometry variation has a major impact on the DC characteristics of the device. Previous works for 22 nm gate length FinFETs [2], [3], and for Si GAA MOSFETs [4] have already investigated this effect.

In this work, we have studied the impact of the device body shape on the electric characteristics of a 10.7 nm SOI-FinFET (dimensions in Table 1) using Sentaurus TCAD simulations. We have used the drif-diffusion model that includes quantum corrections to calibrate the device against Monte-Carlo simulation results [5].

We simulate six different devices, depicted in Fig. 1, each one of them with a slightly different body shape. The changes in the device cross-sections for each device geometry are summarized in Table 2.

We have started with the rectangular cross-section device (A), and keeping constant the height of the body, the oxide width, and the bottom width of the body, we have reduced the width of the top of the body until we reached a triangular cross-section (device F). For every device, we study the main figures of merit that affect SOI-FinFET's performance: threshold voltage (V_{th}), subthreshold swing (SS), on-current (I_{on}), and off-current (I_{off}). These results are shown in Table 3 under two normalization criteria for the current: channel perimeter and channel area, since a change in the cross-section also induces a variation in those two parameters. As expected, the variation in the device geometry has an effect in all figures of merit. As the cross-section of the device moves from a rectangle to a triangle, there is a reduction in the I_{off} for both normalization criteria. This is consistent with the observed increase in V_{th} that ranges from 0.16 V for the device A to over 0.2 V for the device F. When the current is normalized to the perimeter, the I_{on} is larger for the rectangular SOI-FinFET device than for the triangular one (see Fig. 3). However, when the current is normalized to the channel area, the I_{on} remains practically constant. An important requirement in digital devices is a reduced subthreshold swing. In our case, we have found that the more triangular the cross-section is (up to device F) the smaller SS we obtain. This is due to the better control of the gate over the channel transport, since the confinement is stronger for the triangular devices than for the rectangular ones. The reduction of both the I_{off} and the SS indicate that this geometry variation may be beneficial for the behavior of the device during digital switching.

REFERENCES

[1] G. Indalecio, A. García-Loureiro, M. Aldegunde and K. Kalna *Study of statistical variability in nanoscale transistors introduced by LER, RDF and MGG*, Spanish Conference on Electron Devices (CDE) 2013, pp. 95-98

[2] K. Sivasankaran, P.S. Mallick and T.R.K. Kumar Chitroju *Impact of device geometry and doping concentration variation on electrical characteristics of 22nm FinFET*, 2013 IEEE International Conference on Emerging Trends in Computing, Communication and Nanotechnology, pp. 528-531.

[3] R. Fiiacomini and J. Antonio Martino *Trapezoidal Cross-Sectional Influence on FinFET Threshold Voltage and Corner Effects*, Journal of The Electrochemical Society, 2008, pp. H213-H217

[4] I.M. Tienda-Luna, F.J.G. Ruiz, A. Godoy, B. Biel and F. Gamiz *Influence of Orientation, Geometry, and Strain on Electron Distribution in Silicon Gate-All-Around (GAA) MOSFETs*, IEEE Trans. Electron Dev. **58**, no.10, pp. 3350-3357

[5] J. Lindberg, M. Aldegunde, D. Nagy, W.G. Dettmer, K. Kalna, A.J. García-Loureiro, and D. Peri, *Quantum Corrections Based on the 2-D Schrödinger Equation for 3-D Finite Element Monte Carlo Simulations of Nanoscaled FinFETs*, IEEE Trans. Electron Dev., 2014

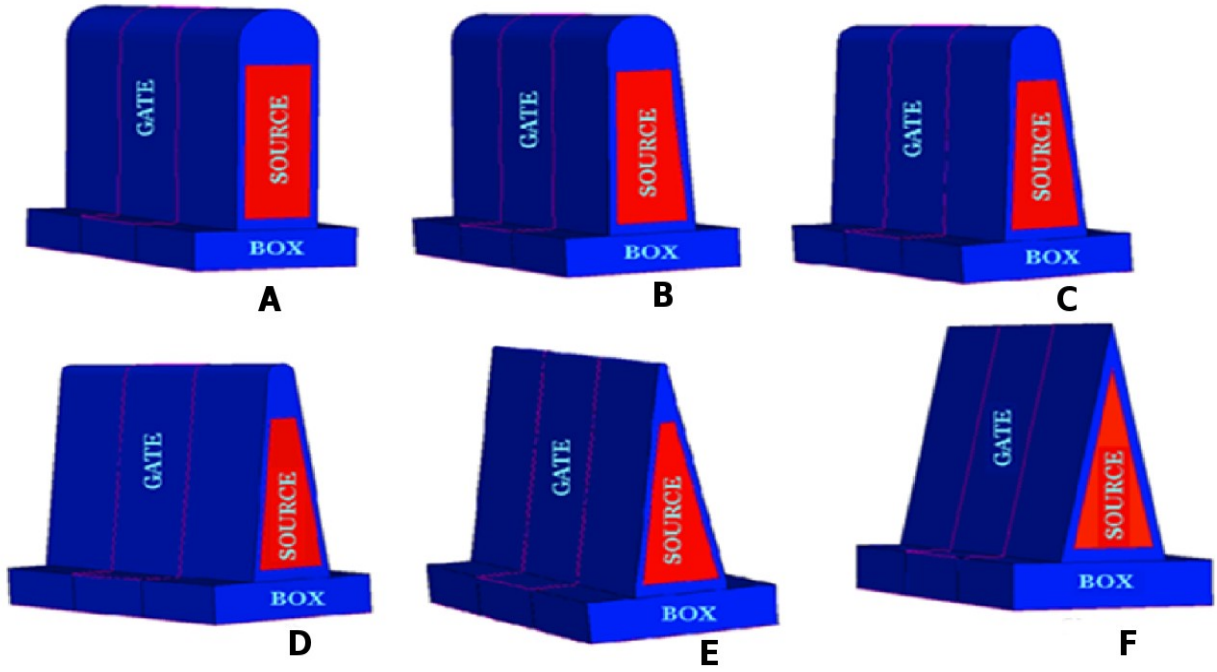

Figure 1: Schematic representation of the six SOI-FinFET geometries being studied

Constant parameters	Value
Supply voltage [mV]	50
Workfunction [eV]	4.32
Gate Length (Lg) [nm]	10.7
S/D doping [cm-3]	1e20
Body Height [nm]	15
Body Width [nm]	5.8
Oxide thickness [nm]	0.725
Gate doping [cm-3]	1e15

Table 1: Device dimensions and parameters for all SOI-FinFET devices

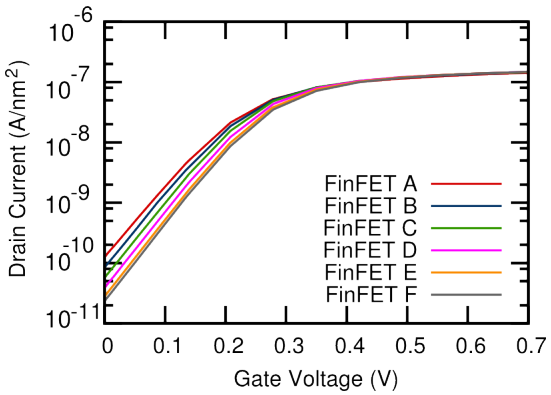

Figure 2: ID-VG characteristics normalized to the channel surface for all the studied device geometries.

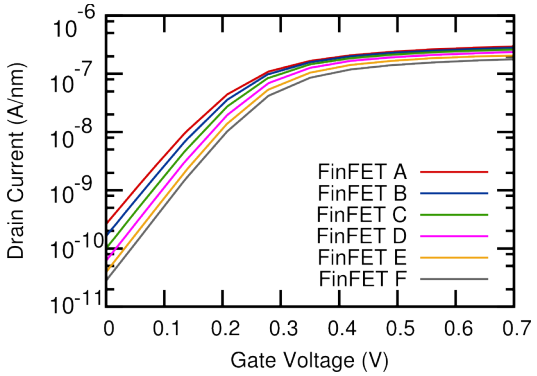

Figure 3: ID-VG characteristics normalized to the channel perimeter for all the studied geometries.

FinFET	Vth [V]	Log_{10}(Ioff [A/nm])	Log_{10}(Ion [A/nm])	SS [mV/dec]
A	0.159	−9.58	−6.53	85.7
B	0.173	−9.78	−6.55	82.8
C	0.186	−9.99	−6.58	80.8
D	0.201	−10.2	−6.63	79.2
E	0.215	−10.4	−6.68	78.4
F	0.230	−10.5	−6.75	78.1
FinFET	**Vth [V]**	**Log_{10}(Ioff [A/nm^2])**	**Log_{10}(Ion [A/nm^2])**	**SS [mV/dec]**
A	0.156	−9.90	−6.85	85.5
B	0.169	−10.1	−6.84	81.9
C	0.181	−10.2	−6.83	80.6
D	0.180	−10.4	−6.83	79.2
E	0.198	−10.5	−6.83	78.3
F	0.203	−10.6	−6.83	77.9

Table 3: Threshold voltage (V_{th}), off-current (I_{off}), on-current (I_{on}) and subthreshold swing (SS) normalized to the channel perimeter (top table) and to the channel area (bottom table) for all the studied device geometries.

Parameters	FinFET					
	A	**B**	**C**	**D**	**E**	**F**
Channel area [nm^2]	87	78.3	69.6	60.9	52.2	43.5
Channel perimeter [nm]	41.6	40.46	39.37	38.32	37.31	36.35
Body top thickness [nm]	5.8	4.64	3.48	2.32	1.16	0

Table 2: Geometry parameters for all the devices