WN and TiN metal gate workfunction variability in a 10.4 nm gate length InGaAs FinFET

N. Seoane[†], G. Indalecio^{*}, E. Comesaña^{*}, M. Aldegunde[†], A. J. García-Loureiro^{*} and K. Kalna[†] [†] ESDC, College of Engineering, Swansea University, UK. E-mail: n.s.iglesias@swansea.ac.uk

* CITIUS, University of Santiago de Compostela, Spain.

III-V FinFETs are serious contenders for high performance digital applications thanks to their high electron mobility and low effective mass. However, as any nano-transistor, their characteristics will be seriously affected by device variability. In this abstract, we present a 3D simulation study of WN and TiN metal gate workfunction variability (MGWV) in the subthreshold region of a 10.4 nm gate length In_{0.53}Ga_{0.47}As FinFET. This device has been designed to meet the 2011 ITRS targets for high-performance logic III-V multigate devices. The dimensions, doping concentrations and nominal device parameters are listed in Table I. The structure has been implemented in a 3D finite element drift-diffusion (DD) device simulator that considers Fermi-Dirac statistics and includes density gradient (DG) quantum corrections [1]. Fig. 1 shows the I_D-V_G characteristics obtained from the 3D DD-DG device simulator calibrated against Silvaco's 3D ballistic non-equilibrium Green's function (NEGF) simulations at both low and high drain biases. The simulations have been carried out considering metal gate workfunction (MGW) induced variability in WN and TiN gate InGaAs FinFETs, studying four average grain sizes (GS) (10, 7, 5 and 3 nm). Results are based on statistical samples of 300 devices at $V_D=0.05$ V. To model the dependence of the MGW on the granularity, we follow the methodology described in [2]. The work function of both metal gates was set to 4.7 eV. Fig. 2 shows an example of the WN (a) and TiN (b) gate workfunction distributions due to MGWV, for a 5 nm average grain diameter. WN has four possible grain orientations with MGWs between 5.4 and 4.3 eV, while TiN has only two possible grain orientations with MGWs of 4.6 and 4.8 eV[3]. Fig. 3 shows the V_T , SS, and $log_{10}(I_{off})$ standard deviations due to the MGWV as a function of GS and the type of metal. For both metal gates, the standard deviation of the three figures of merit decreases with a reduction in GS. A decrease in GS from 10 nm to 3 nm reduces the spread in V_T and $\log_{10}(I_{OFF})$ by approximately 3 times. The WN metal gate gives extremely large MGWV in characteristics (with σV_T around 120 and 40 mV when GS are 10 and 3 nm, respectively) as compared to the TiN metal gate (σV_T are 41 and 14 mV for GS 10 and 3 nm, respectively). This is due to the span of 1.1 eV in the workfunctions of the different grain orientations (much larger than the 0.2 eV span for the TiN), which may prove WN to be unsuitable for application in III-V FinFETs. An equivalent gate length TiN metal-gate SOI Fin-FET [4] has the σV_T slightly larger for 10 and 5 nm grain sizes than that observed for the III-V FinFET (see Fig. 3). Figs. 4, 5 and 6 show the normal quantile-quantile (Q-Q) plots of the V_T, SS and $log_{10}(I_{off})$ distributions, respectively, compared to theoretical quantiles from the normal distribution (black lines). For both metal gates, the Q-Q plots are close to a Gaussian distribution when GS is small. As GS increases, the plots move away from a Gaussian distribution in the tails and there is an increase in the slope (related to the increase in the σ of the distribution). This is reflected, for the TiN metal gate, in a saturation in the V_{T} and $\log_{10}(I_{off})$ values at the tails, and in a shift from the theoretical quantiles in the SS at the centre of the distribution. Since the TiN metal only has 2 different possible orientations, the distribution will be closer to bimodal when GS is large (behaviour not observed for the WN metal grains).

References

- [1] N. Seoane, et al., Solid-St. Electron., 69, 43, (2012).
- [2] G. Indalecio, et al., SISPAD, 149 (2012).
- [3] S. H. Rasouli, et al., ICCAD, 714 (2010).
- [4] X. Wang, et al., IEDM Tech. Dig., 103 (2011).

TABLE I

DIMENSIONS, DOPING CONCENTRATIONS AND NOMINAL DEVICE PARAMETERS FOR THE SIMULATED DEVICE.

Symbol	Value	Description
$L_G(nm)$	10.4	Physical gate length
EOT(nm)	0.59	Equivalent oxide thickness
$W_{fin}(nm)$	6.1	Fin width
$H_{fin}(nm)$	15.2	Fin heigth
$N_c(cm^{-3})$	10^{17}	P-type channel doping
$L_{SD}(nm)$	10.4	Length of n-doped S/D regions
$N_{SD}(cm^{-3})$	$5x10^{19}$	Peak value S/D doping
$\delta_{SD}(nm)$	1.85	Gaussian decay S/D doping
$V_T(mV)$	23.0	Threshold voltage
$I_{off}(nA/\mu m)$	44.4	Off-current with $V_G=0.0 V$
SS(mV/dec)	78.3	Subthreshold slope



Fig. 1. I_D - V_G characteristics comparing 3D quantum corrected DD simulations (DD-DG) to NEGF Silvaco simulations.



Fig. 2. Example of WN (a) and TiN (b) MGWV for GS=5 nm.



Fig. 3. V_T , SS and $\log_{10}(I_{OFF})$ standard deviations due to MGWV as a function of the GS and the metal gate. σV_T for a TiN metal-gate SOI FinFET [4] is also shown for comparison.



Fig. 4. Quantile-quantile (Q-Q) plots of the V_T distribution due to MGWV for the WN (top) and TiN (bottom) metal gates.



Fig. 5. Q-Q plots of the SS distribution due to MGWV for the WN (top) and TiN (bottom) metal gates.



Fig. 6. Q-Q plots of the I_{OFF} distribution due to MGWV for the WN (top) and TiN (bottom) metal gates.