Predictivity of the non-local BTBT model for structure dependencies of tunnel FETs

Koichi Fukuda, Takahiro Mori, Wataru Mizubayashi, Yukinori Morita,
Akihito Tanabe, Meishoku Masahara, Tetsuji Yasuda, Shinji Migita, and Hiroyuki Ota
Collaborative Research Team Green Nanoelectronics Center (GNC),
National Institute of Advanced Industrial Science and Technology (AIST)
16-1 Onogawa, Tsukuba, Ibaraki 305-8569, JAPAN

ABSTRACT

Device simulation with the non-local band to band tunneling model is evaluated for the tunnel-FET modeling focused on their geometry effects. Measured characteristics of SOI, Fin, and parallel-plate tunnel FETs fabricated in our group are compared with simulations. The non-local model explains the various geometry effects very well throughout the comparisons. Validity of the non-local model is now ensured for the device design of tunnel FETs.

INTRODUCTION

For the modeling of tunnel FETs (TFETs), the non-local band to band tunneling (BTBT) model is widely used. However, its limitation for the TFET modeling is not clarified yet. Our group has already published varieties of TFETs, such as SOI, Fin, and parallel-plate (PP) TFETs. These experiments offer good chances to evaluate the model limitation.

MODEL

Kane's formula (1) has been widely used for PN junction leakage analyses in device simulators.

$$G_{BTBT} = A \cdot E^{\gamma} \cdot \exp(-B/E) \quad (1)$$

In the non-local model, electric field E is substituted by the non-local definition in order to consider the non-linear band bending. The authors have implemented the non-local model [1] in the three-dimensional device simulator HyENEXSS [2], where conduction and valence bands are traced to evaluate the minimum tunnel path lengths as explained in Fig.1.

RESULTS

Fig.2 shows variety of TFETs fabricated in our group, SOI[3], Fin[4], and PP[5] TFETs. These TFETs have geometrically different features and are good choice for model evaluations.

Fig.3 shows I_D-V_G characteristics of an SOI p-type TFET compared with simulation results. In the measured curve, gate leakage currents are observed around $V_G=0V$ not included in the simulation. Other regions are sufficiently explained by the non-local model even in the off state region $V_G>0$, where gate induced drain leakage is occurred at the drain side.

Fig.4 shows I_D-V_D characteristics of an SOI p-type TFET compared with simulation results. The V_G dependence and the current saturation are different from those of MOSFETs, and both are well explained by the model.

Fig.5 shows the back-gate bias dependencies of threshold shifts of dual-gate Fin p-type TFETs with Fin-thicknesses as parameters [4]. Even with their complexities of Fin-shapes and doping profiles, basic physics are well explained by the simple device simulation results.

Fig.6 shows I_D *vs* L_{OV} of the PPTFETs which enhance the tunnel currents at the source-gate overlap regions suggested by our group [5]. The non-linear relationships of measured I_D *vs* L_{OV} are well reproduced by the model.

CONCLUSION

Through varieties of TFETs experiments, the non-local BTBT model is proved to be a generic and useful tool for TFETs including various geometry effects.

ACKNOWLEDGMENT

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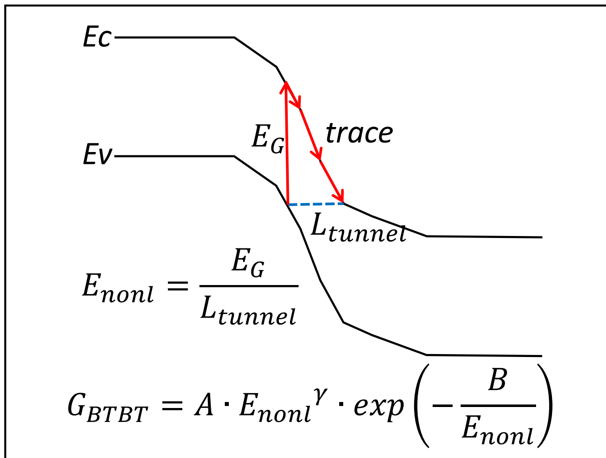

Fig. **1**. Concept of our implementation of the non-local BTBT model. Conduction and valence bands are traced to find the tunnel path length. [1]

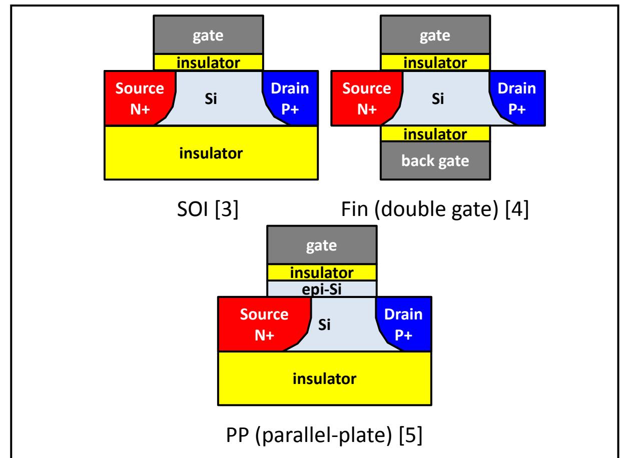

Fig. 2. Experimental results of SOI [3], Fin [4], and PP [5] (parallel-plate) types of TFETs are discussed in this work.

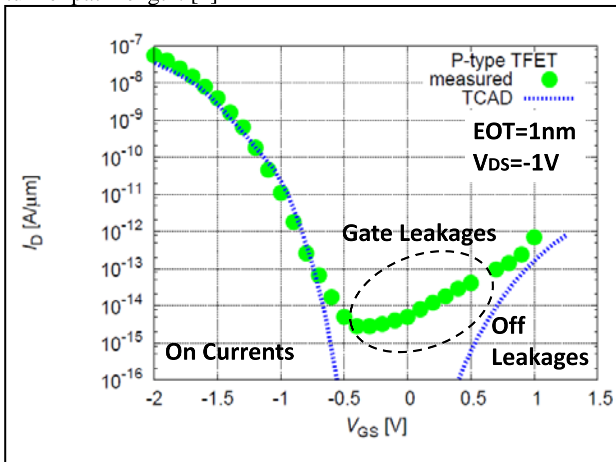

Fig. 3. I_D-V_G characteristics of SOI-TFET compared with measurements. Gate leakages are observed in dashed line area of measurements. Both on/off currents are well explained.

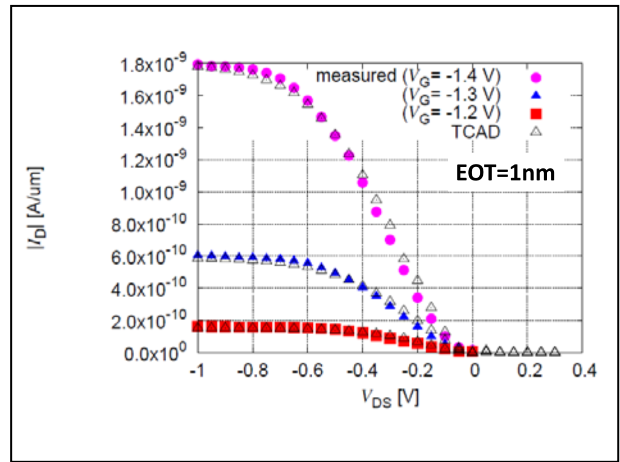

Fig. 4. I_D-V_D characteristics of SOI-TFET compared with measurements. Good accuracy is obtained.

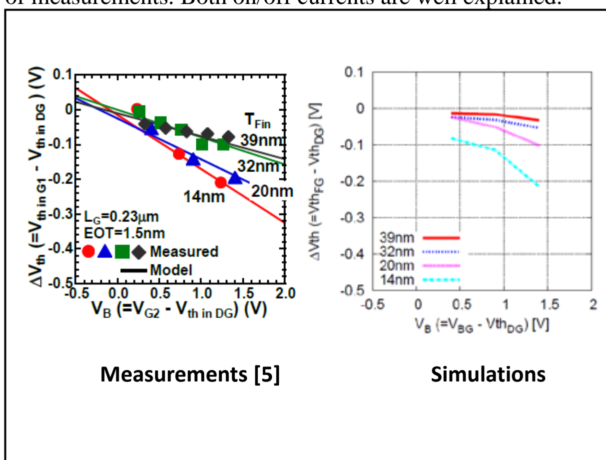

Fig. 5. Back-gate bias dependencies of threshold voltage shifts of dual-gate Fin TFETs, measurements (left) and simulations (right).

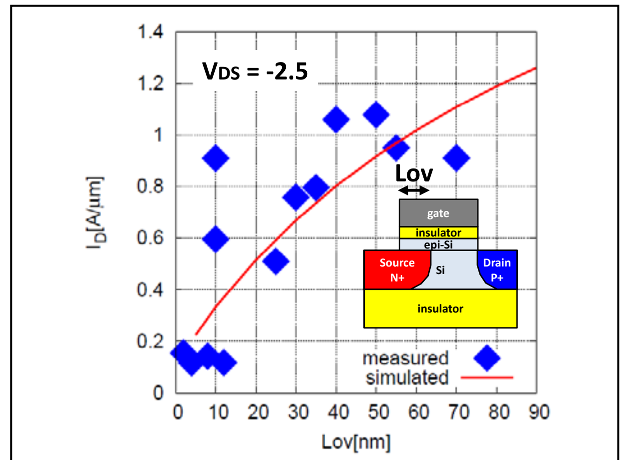

Fig. 6. Overlap length dependencies of drain currents of PP-TFETs. Simulation explains the non-linear dependence of the experimental results.