Self-Heating Effects in nanowire Depletion Mode Junctionless Transistor

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Thermal management and power dissipation issues in microprocessors are quickly emerging as the ultimate bottleneck to improving the performance of consumer/commercial electronics. Controlling device temperature and power dissipation is a key to sustaining electronic devices with longer battery life and improves the overall device reliability and life expectancy. As such, thermally conscious blueprints has become in recent years the focal concern of semiconductor roadmaps, at all design phases, as the temperature at the chip level and within a single transistor rises for future electronic devices [1,2]. Without proper thermal management, inordinate power dissipation can potentially bring to end integrated circuit functionality. In this regard, there is substantial interest in designing simulation tools which thoroughly couple accurate electrical and thermal transport models

In this paper we employ a 3D full band Monte Carlo simulator with 2D quantum correction coupled self-consistently to the phonon Monte Carlo model introduced [3] to examine the electrothermal transport of junctionless Multigate MOSFET. The full self-consistent two-way coupling of electron and phonon populations is achieved in two steps added to the standard electron and phonon Monte Carlo simulations. The first step consists of furnishing the heat generation data obtained from our 3D quantum corrected Monte Carlo to a phonon Monte Carlo which subsequently dissipates the anharmonic phonon processes utilizing the full phonon dispersion. This first step is the forward or dissipation portion of the two-way coupling. The second step in the two-way coupling process is the feedback from the thermal phonon simulator back to the electron Monte Carlo. This second step is achieved by finding a temperature field from the phonon particle densities and energies and then utilizing that temperature map to update the temperature-dependent electron-phonon scattering rates. A key advantage of our 3D electro-thermal simulator is that it provides an accurate description of the spatial variation of self-heating and its effect in nonequilibrium carrier dynamic which influences device performance. The temperature hot spots, current degradation, and transport coefficients can be engineered to yield optimal design (maintain power dissipation and current drive within tolerable level).

Figure 1 demonstrates that only thin cross-sections yield acceptable I_{off} current, leading to requiring that silicon channels must be thin enough to have (at zero gate voltage) a high energy barrier between source and drain along the whole cross-section of the device. Furthermore, even for the thinnest structure (T_{si} = 5 nm), the doping concentration must be lower than $4x10^{19}$ cm^{-3}. Figure 2 shows the temperature profile representative of a junctionless transistor. The temperature peak is significantly lower than the one measured for SOI multi-gate MOSFET devices with similar dimensions

References

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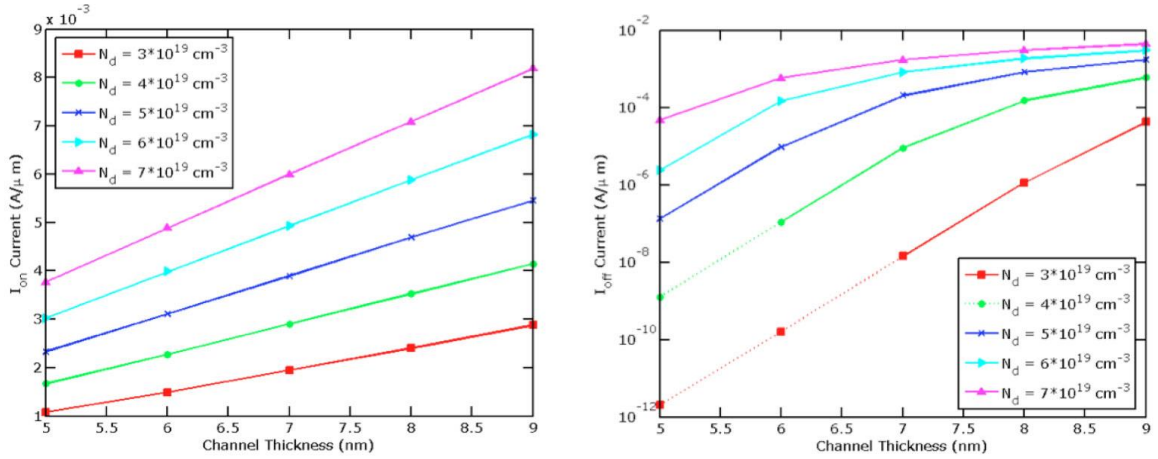

Figure 1: I_{on} (left) and I_{off} (right) current of junctionless transistors as a function of channel thickness and doping concentration. L_G = 20 nm; VG = VD = 1.2 V.

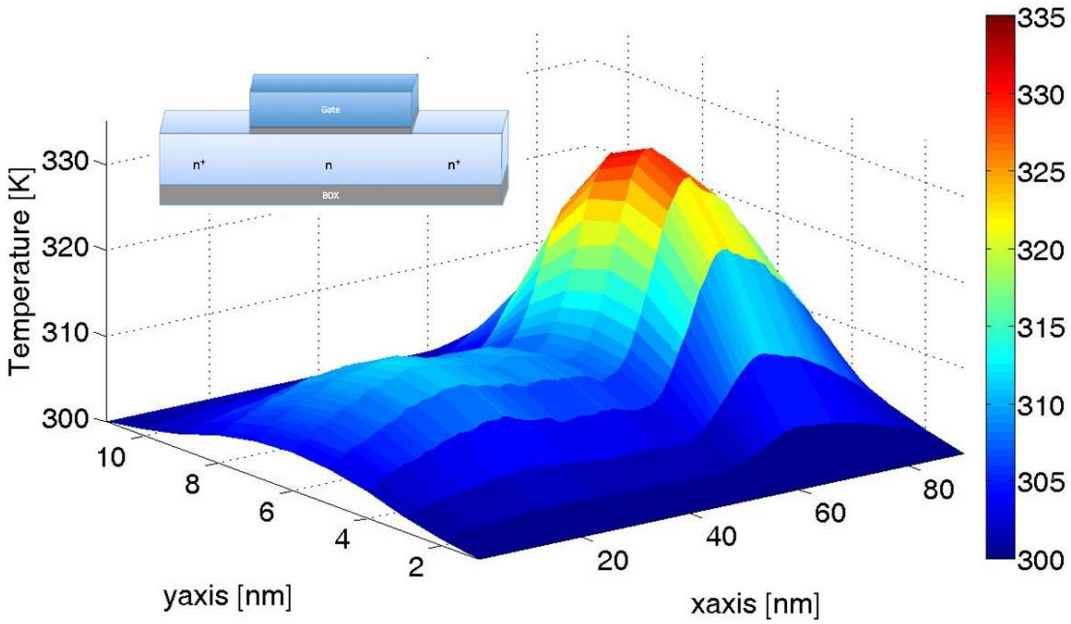

Figure 2: Temperature profile of a junctionless transistor with a 5nm square cross-sectional length and L_G= 20 nm. Inset: Schematic of a junctionless transistor.