Uncovering the Temperature of the Hotspot in Nanoscale Devices

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As we scale semiconductor devices towards the nanometer scale, there are a variety of phenomena that affect device performance including *spatial fluctuations*, *temporal fluctuations* and *self-heating effects*. *Self-heating* occurs in nanoscale devices because of the fact that voltages do not scale proportionally to device size thus leading to hot electrons that give up their energy very quickly, mostly to the optical phonon bath and some energy to the acoustic phonons. The zone center optical phonons having almost zero group velocity do not transport the heat and a hot spot forms. Eventually the optical phonon energy is being transported through the system by an unharmonic decay processes in which optical phonons decay into multitude of acoustic phonons that dissipate the heat through the system. Understanding what is the value of the hotspot temperature still remains an issue as direct measurements are not possible.

In this work we demonstrate: 1) that we can co-simulate multiple devices with our thermally coupled Monte Carlo device simulator [1]; and 2) that the synergy of experiment and theory can give quite accurate values for the temperature of the hot-spot in conventional planar MOSFETs.

The experimental procedure is as follows. First, as schematically illustrated in Fig. 1, we extract the temperature increase ΔT induced by a nFET (i.e. the "heater" from Fig. 1) by making use of a nFET sensor that is located very nearby this nFET device under test (DUT). This is done using the sensor's *temperature dependent characteristics.* The sensor is connected in the example to a common source configuration with the heater (Fig. 1(a)). This configuration allows the closest possible 'in silicon' sensor, as the devices are only separated by one gate pitch and share the same active area, surrounded by shallow trench isolation [Fig 1(b)]. Subsequently, the sensor's subthreshold swing (SS) is *extracted using modified EKV model* [2].

As a calibration, the external temperature is ramped and the SS shows linear dependency over a wide temperature range, with a temperature dependency of about 2.85 mV/dec/K (Fig. 2(a)), similar to [3]. Subsequently, nFET heater is biased in variable saturation conditions (high V_D and V_G). The subthreshold swing reduction in the sensor is found to be proportional to the heat dissipated in the device [Fig. 2(b)]. The ΔT and R_{TH} of these devices can therefore be extracted for the varying operating zones [Fig. 2(c)]. Knowing the temperature of the sensor, the next step is to perform device simulations that produce the average lattice temperature profile in the device. The average lattice temperature in the sensor for given input power has to match the experimentally extracted value of the temperature.

It is important to note that in the theoretical modeling of the experimental set-up from Fig. 1 we solve the 2D Poisson equation self-consistently with a Monte Carlo transport kernel and a 2D energy balance equations solvers for the acoustic (lattice) and optical phonon baths [1], thus moving away the commonly used Joule heating model used in commercial device simulators. Such simulations give rise to more pronounced hot-spots, because they accurately represent the optical to acoustic phonon bottleneck.

There are two possible configurations that achieve this goal. One is common source (CS) and the other one is common drain (CD) configuration. Simulation results for the lattice temperature profile and the average lattice temperature profiles along the channel are shown in Figure 3. It is clearly seen from the results presented that the magnitude of the hot-spot is larger in the common source configuration.

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Acknowledgements
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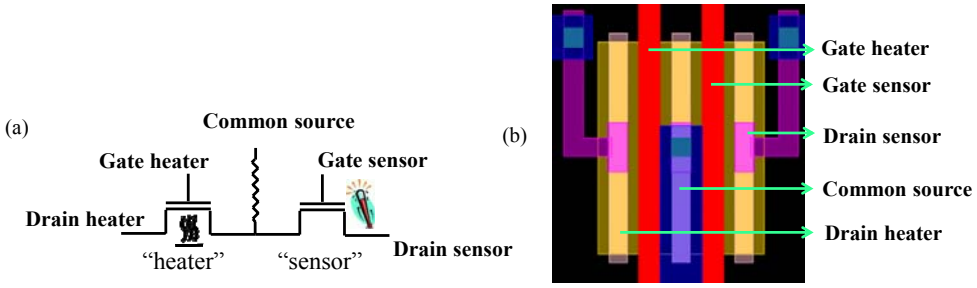

Fig. 1. (a) Two nFETs have common source connecting, can operate in a saturation and subthreshold, respectively. The structure exists for varying gate lengths and device to device pitches. (b) Mask image indicating both FETs being located in a common active area, spaced by only one poly pitch.

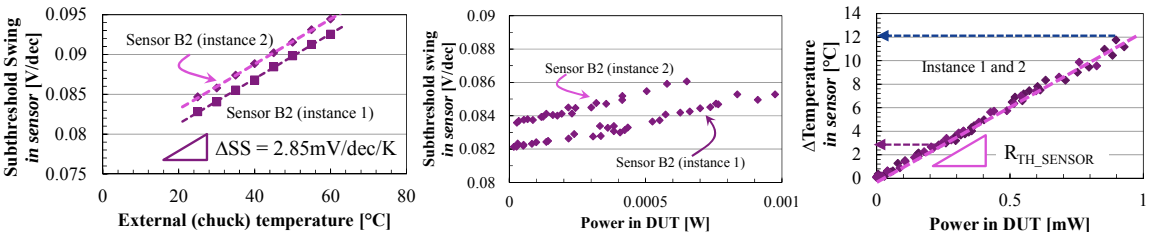

Fig. 2. Results for two instances of a device (Fig 1). (a) The subthreshold swing (SS) varies linearly with the externally applied chuck temperature. (b) When drawing a large current through the heater, the SS of the sensor varies linearly. (c) Using the initial SS as a reference, the extracted ΔT in the sensor gives consistent results for both instances.

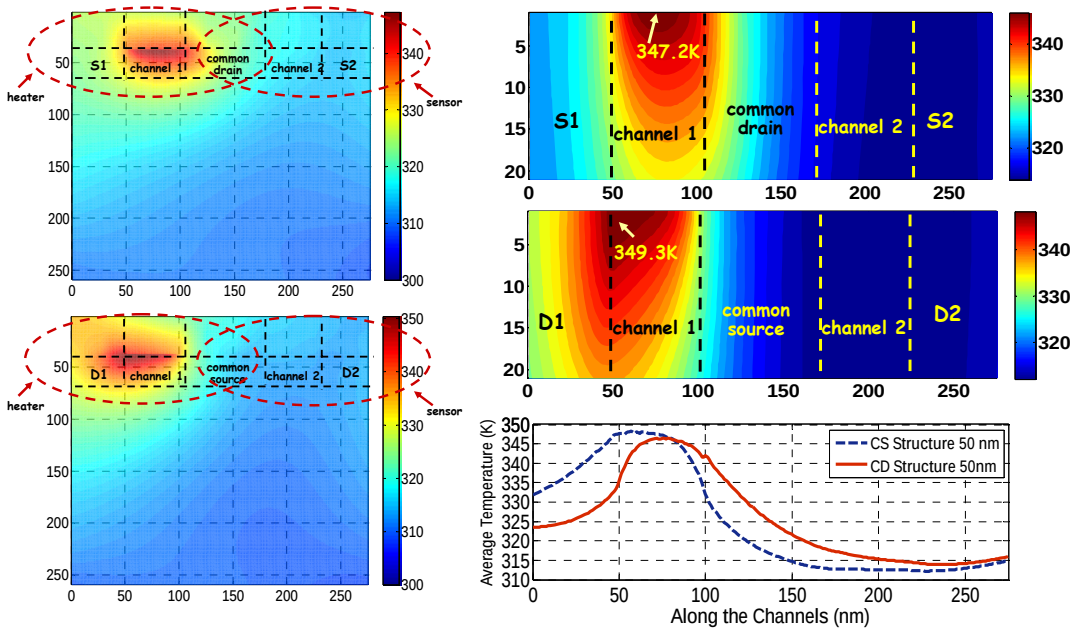

Fig. 3. Left: Lattice temperature profile for CD (top) and CS (bottom) configurations. Right: Lattice temperature profile in the active silicon layer for the two simulated structures. Average lattice temperature profile in the active silicon layer (bottom right). Multi-scale approach has been used in obtaining these results. The complete circuitry was modelled using COMSOL simulations and the boundary conditions for the active devices region was used in the thermal Monte Carlo device solver.

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