Two-Dimensional Self-Consistent Simulation on Program/Retention Operation of Charge Trapping Memory

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INTRODUCTION

Silicon-nitride- or high-κ-material-based charge trapping memories (CTM) are considered to be the most promising candidates for the NAND structures, due to their immunity to stress-induced leakage current and reduced coupling capacitance, especially in stackable 3D architectures[1,2]. Accurate simulation of the CTM is important to the design and optimization of its memory performance and reliability issues. With the development of 3D NAND structures, simulation of the charge behavior in 2D is the key issue to investigate the performance and reliability of 3D CTM. Most of the CTM simulators perform 1D simulation of the charge behavior along the gate stack vertical to the channel[3-5]. However, few work deal with charge behavior in 2D. In this paper, a 2D self-consistent numerical simulator is developed with the incorporation of major physical models to study the programming and retention performance in 2D with non-uniformly distributed traps.

MODELS AND NUMERICAL TREATMENT

Fig.1 plots the simulation structure and area. Mechanisms involved during programming and retention of memory cells are schematically depicted in Fig. 2(a) and Fig. 2(b) respectively. For the purpose of modeling these physical mechanisms and describing the transport of charged carriers through the gate stacks, a set of 2D non-linear partial differential equations is solved in our simulator, comprising the 2D Poisson equation, the 2D carrier continuity equation with the drift-diffusion transport scheme and the trapped charge conservation equation accounting for the trapping/ detrapping dynamics, which are outlined as follows:

$$\vec{\nabla}\cdot\left(\varepsilon\,\vec{\nabla}\varphi\right)=q(n_f+n_t) \quad (1)$$

$$\frac{\partial n_f}{\partial t}=\frac{1}{q}\vec{\nabla}\cdot\vec{J}_n-c_n(N_T-n_t)n_f+e_n n_t \quad (2)$$

$$\frac{\partial n_t}{\partial t}=(c_n n_f+r_{BT})(N_T-n_t)-(e_n+r_{TB})n_t \quad (3)$$

where q is the electronic charge, ε is the material dielectric constant, N_T, n_t, and n_f are volume density of traps, trapped carriers and free carriers, c_n is the free-carrier capture coefficient calculated by the Shockley-Read-Hall (SRH) theory[6], e_n is the trapped-carrier emissivity contributed by thermal and the Poole-Frenkel process[7], r_{BT} and r_{TB} are Band-to-Trap (BT) tunnelling and Trap-to-Band (TB) emission rate respectively, computed using the Wentzel–Kramers–Brillouin (WKB)[8] approximation.

The simulation flowchart to self-consistently solve the equation set is illustrated in Fig. 3. The current density is discretized by the Scharfetter-Gummel[9] scheme, which can afford greater accuracy with fewer nodes and larger time-steps. The implicit method is utilized to ensure time stability. To verify the simulator, device with gate stack composed of SiO_2(4nm)/Si_3N_4 (8.7nm)/Al_2O_3(11.5nm) is simulated and compared with the experiment data[3]. The parameters used during the simulation is listed in Table 1. As shown in Fig.4, the results indicate that our simulator can well reproduce the experiment data.

RESULTS AND DISCUSSION

Fig. 5 shows the trapped electrons occupation rate along vertical direction from tunneling oxide interface to blocking oxide interface of the above-mentioned device. Fig.6 reveals that TB tunneling is the major charge loss mechanism at room temperature (300K) in device with gate stack composed of SiO_2(4nm) /Si_3N_4(8.7nm)/Al_2O_3(11.5nm), while thermal emission dominates at high temperature (400K). In addition, the comparison between evolutions of trapped electrons under different retention temperature is demonstrated in Fig. 7, which further elucidates that TB tunneling through gate oxide is the primary cause of charge loss at room temperature and tunneling out through blocking oxide governs the retention characteristics at high temperature. Fig. 8 exhibits the execution time of each solver with respect to different number of vertices. The performance under large vertex number is acceptable, enabling the simulator to analyze memory structures of 3D applications.

CONCLUSION

A 2D self-consistent numerical simulation approach with drift-diffusion transport scheme for charge trapping memories under program/retention operations is developed, aiming to investigate memory devices in scaled structures and especially in 3D applications.

ACKNOWLEDGMENT

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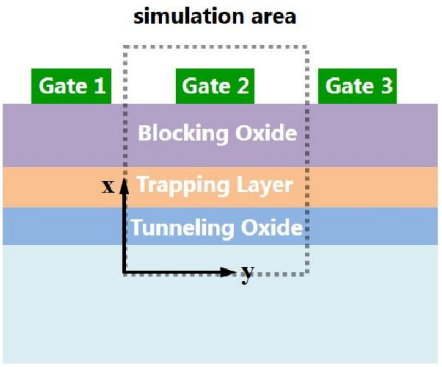

Fig.1 The schematic of charge trapping device and the simulation area.

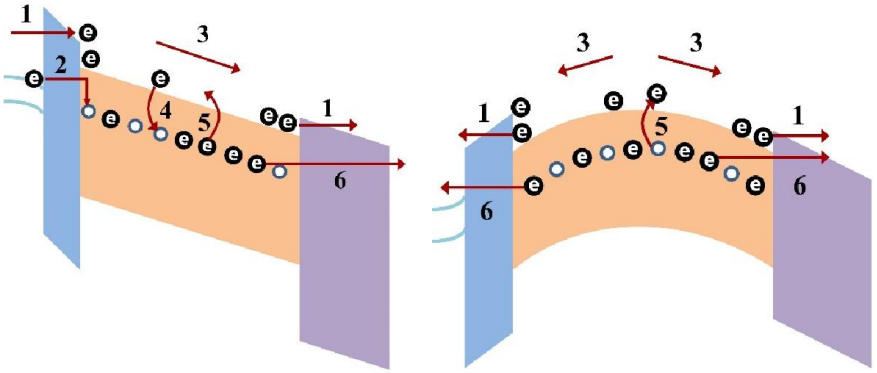

Fig. 2 Dominant physical mechanisms involved in (a) programming and (b) retention operations. These models are: 1-DT/FN (or MFN) tunneling, 2-Band-to-Trap tunneling, 3-drift and diffusion transport in the trapping layer, 4-carrier capture process, 5-carrier emission process (including thermal and Poole-Frenkel emssion) and 6-Trap-to-Band tunneling.

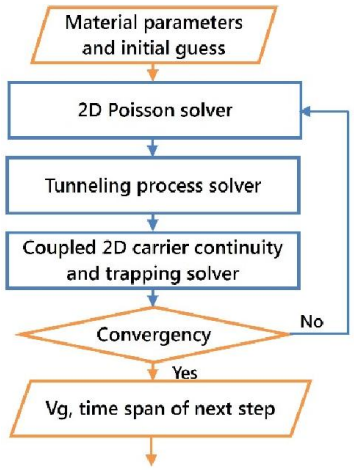

Fig.3 Simulation flowchart of the coupled equations.

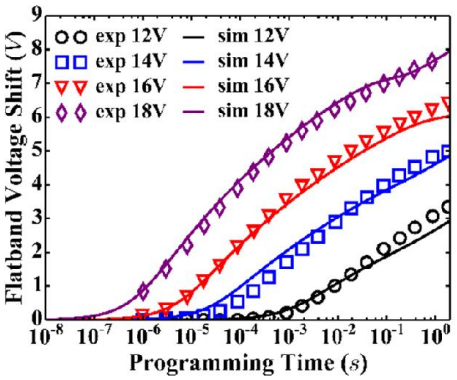

Fig. 4 Reproduction of experiment data under different programming bias for memory device with SiO_2(4nm)/Si_3N_4 (8.7nm)/Al_2O_3(11.5nm) gate stack.

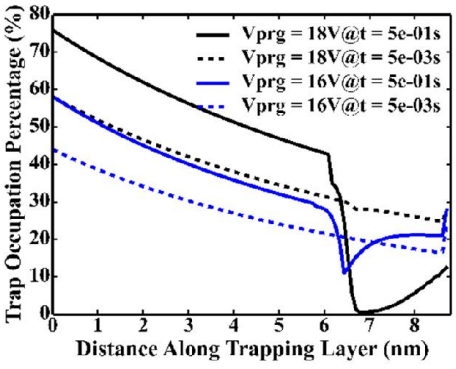

Fig.5 Trapped electrons occupation rate along the direction from tunneling to blocking oxide interface in device with SiO_2(4nm)/Si_3N_4(8.7nm)/Al_2O_3(11.5nm) gate stack.

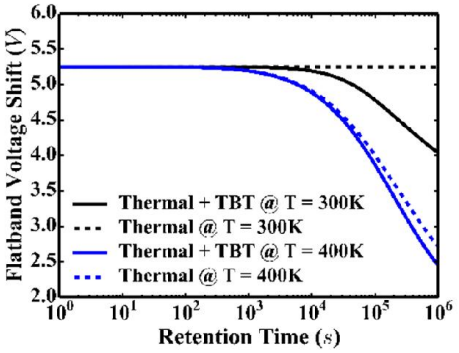

Fig.6 Influence of Thermal emission and TB tunneling on memory retenion of device with SiO_2(4.5nm)/Si_3N_4(7nm)/Al_2O_3(12nm) gate stack.

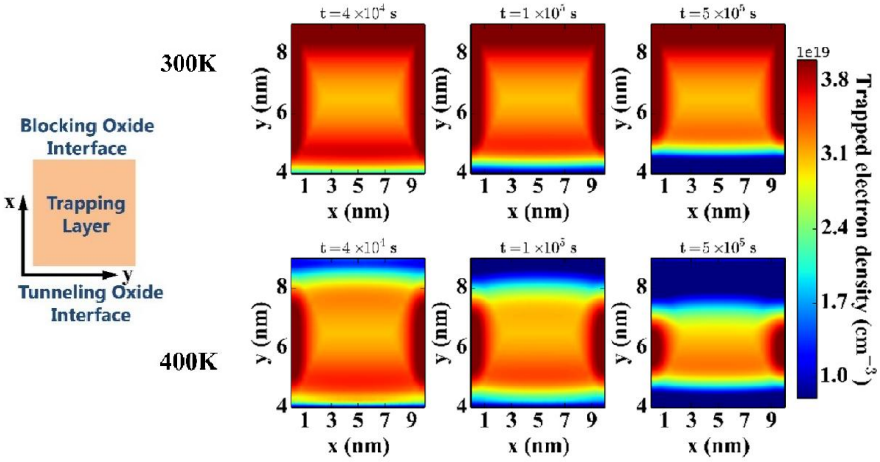

Fig.7 Time evoluation of trapped electrons under different retention temperature for device with SiO_2(4.5nm)/Si_3N_4 (7nm)/Al_2O_3(12nm) gate stack and width of 10nm.

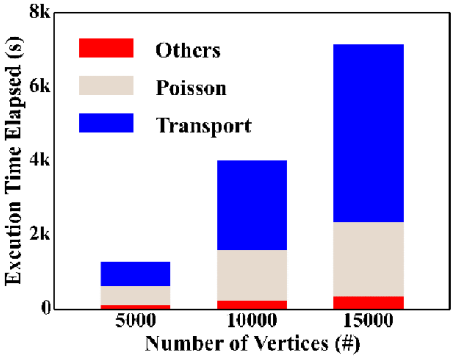

Fig .8 Execution time of the simulator measured on 2×CPU@3.0GHz.

Table 1 Main parameters in the simulation

Parameter	*Value*	*Parameter*	*Value*
SiO_2 effective mass	0.40 m_o	Si_3N_4 trap density	7×10^{19}cm^{-3}
Al_3O_2 effective mass	0.20 m_o	Si_3N_4 electron mobility	0.1cm^2/V/s[5]
Si_3N_4 effective mass	0.42 m_o	Si_3N_4 TBT frequency	1×10^7Hz[4]
Si_3N_4 trap crosssection	2×10^{-14}cm^{-2}	Si_3N_4 trap energy	1.9eV