3D Finite Element Schrödinger Equation Corrected Monte Carlo Simulations of Nanoscale FinFETs

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3D FinFET multi-gate technology [1] established itself as the next solution for CMOS scaling into sub-22 nm digital technology [2]. This scaling is strongly affected by the exact device geometry and architecture [3] since the fabrication of non-planar transistors result in very unique shapes. This brings new serious challenges for physically based device modelling [4]. However, these irregular geometries can be accurately described by 2D Schrödinger equation quantum corrected Monte Carlo (MC) toolbox [5] based on a 3D finite element (FE) method thanks to finding solutions to the problem of self-forces in the FE MC device simulations [6]. In this work, we report nanoscale n-channel Si SOI FinFETs with three different shapes: rectangular (REC), wide- (WTRI) and narrow-triangular (NTRI) including rounded corners [7] simulated by the 3D MC including influential impact of the interface roughness (IR) [6].

The 3D device mesh contains predefined 2D planes perpendicular to the transport x-direction as illustrated in Fig. 1. 2D electrostatic potential, $V(y,z)$, acquired on the planes from $V(\mathbf{r})$, enters the 2D Schrödinger equation:

$$-\frac{\hbar^2}{2}\nabla_\perp \cdot \left[(\mathbf{m}^*)^{-1} \cdot \nabla_\perp \psi(y,z)\right] + U(y,z)\psi(y,z) = E\psi(y,z), \quad (1)$$

where E is the energy, $(\mathbf{m}^*)^{-1}$ is the inverse effective mass tensor, $\psi(y,z)$ is the wavefunction penetrating into the surrounding oxide, and $U(y,z) = -[qV(y,z) + \chi(y,z)]$ is the potential energy with $\chi(y,z)$ being the electron affinity. Note that Eq. 1 is solved entirely on a 2D FE mesh defined by the planes (Fig. 1) to speed-up the simulations [5]. The 2D quantum density n_{q} is interpolated onto the 3D domain to obtain a 3D quantum correction potential as [8] $V_{\mathrm{qc}}(\mathbf{r}) = (k_{\mathrm{B}}T/q)\log\ [n_{\mathrm{q}}(\mathbf{r})/n_{\mathrm{ien}}(\mathbf{r})] - V(\mathbf{r}) + \phi_n(\mathbf{r})$, where $n_{\mathrm{ien}}(\mathbf{r})$ is the effective intrinsic carrier concentration and $\phi_n(\mathbf{r})$ is the quasi-Fermi electron potential. The particles move in the quantum corrected potential according to $\mathrm{d}\mathbf{k}/\mathrm{d}t = (q/\hbar)\nabla\left[V(\mathbf{r}) + V_{\mathrm{qc}}(\mathbf{r})\right]$ [8].

Table I lists the dimensions for the REC, WTRI and NTRI device shapes illustrated in Figs. 5, 6, and 7, respectively. Fig. 2 shows the deep sub-threshold on a log scale from the drift-diffusion (DD) simulations. Fig. 3 shows the $\mathrm{I_D}$-$\mathrm{V_G}$ characteristics normalized by the perimeter and Fig. 4 when normalized by the area at high drain bias. Two channel orientations are simulated: $\langle 100\rangle$ and $\langle 110\rangle$. The REC shape performs best followed by the WTRI and the NTRI when normalized-to-perimeter. The NTRI outperforms both the WTRI and the REC when normalized-to-area. The drive current for both normalizations, the calculated drain induced barrier lowering (DIBL) and sub-threshold slope (SS) are collected in Table II. Figs. 5-7 show electron density in cross-sections for the three shapes at $\mathrm{V_G}$-$\mathrm{V_T}$ =0.7 V and $\mathrm{V_D}$ =0.7 V in the middle of the gate.

In summary, both TRI shape FinFETs can deliver outstanding performance in the sub-threshold and in the on-region. However, the on-current is limited by the total carrier density passing through the channel (the impact of interface roughness scattering is rather restricted) determined by the confinement which, in turn, has to be correctly modelled using Schrödinger based quantum corrections, especially, at high drain biases.

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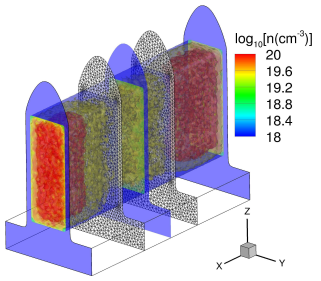

Fig. 1: Iso–surface of the electron density from the 2D Schrödinger solver at V_G-V_T = 0.7 V, V_D = 0.7 V and slices across the channel in the 10.7 nm gate length rectangular shape FinFET.

Technology [nm]	REC	WTRI	NTRI
Height [nm]	15	21.21	17.67
Width [nm]	5.8	5.8	5.8
Perimeter [nm]	35.8	35.8	35.8
Area [nm^2]	87	74	51

TABLE I
DEVICE DIMENSIONS AND PARAMETERS: FINFET HEIGHT AND WIDTH, CIRCUMFERENCE OF THE CHANNEL, AND AREA OF THE DEVICE CROSS-SECTIONS.

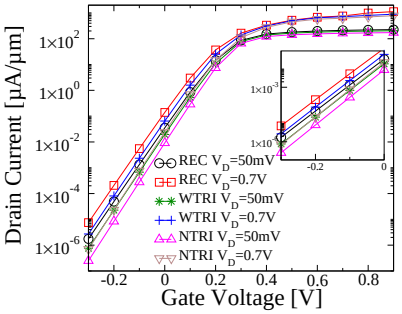

Fig. 2: I_D-V_G characteristics from the DD simulations at V_D = 0.05 V and 0.7 V using a normalised-to-perimeter current for the rectangular (REC), wide- (WTRI) and narrow-triangular (NTRI) shaped FinFETs.

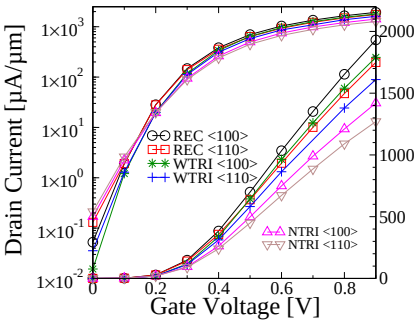

Fig. 3: I_D-V_G characteristics at V_D = 0.7 V using a normalised-to-perimeter current for the rectangular (REC), wide- (WTRI) and narrow-triangular (NTRI) shaped FinFETs for the ⟨100⟩ and ⟨110⟩ channels.

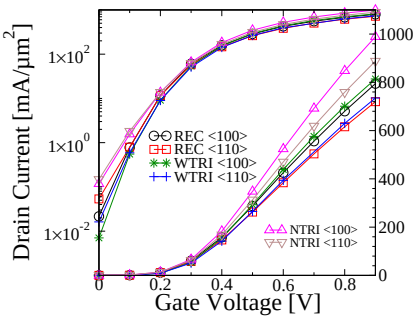

Fig. 4: I_D-V_G characteristics at V_D = 0.7 V using a normalised-to-area current for the rectangular (REC), wide- (WTRI) and narrow-triangular (NTRI) shaped FinFETs for the ⟨100⟩ and ⟨110⟩ channels.

Technology [nm]	REC	WTRI	NTRI
SS_{LOW} [mV/dec]	70	68	66
SS_{HIGH} [mV/dec]	71	69	66
$DIBL_{MC}^{\langle 100\rangle}$ [mV/V]	65	55.3	60
$DIBL_{MC}^{\langle 110\rangle}$ [mV/V]	65	57	64
$I_{MC}^{\langle 100\rangle}$ [μA/μm]	1930	1790	1436
$I_{MC}^{\langle 110\rangle}$ [μA/μm]	1749	1610	1290
$I_{MC}^{\langle 100\rangle}$ [μA/μm^2]	794	814	989
$I_{MC}^{\langle 110\rangle}$ [μA/μm^2]	720	735	888

TABLE II
SUB-THRESHOLD SLOPE (SS) AT V_D = 0.05 V AND 0.7 V FROM THE DD, DIBL FROM MC, AND DRIVE CURRENTS ($I_{MC}^{\langle \text{channel orientation}\rangle}$) FOR RECTANGULAR (REC), WIDE- (WTRI) AND NARROW-TRIANGULAR (NTRI) FINFETS.

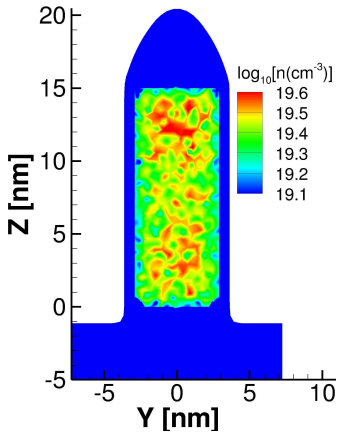

Fig. 5: Electron density in a cross-section through the middle of the gate in the rectangular ⟨100⟩ channel FinFET at V_G-V_T = 0.7 V, V_D = 0.7 V.

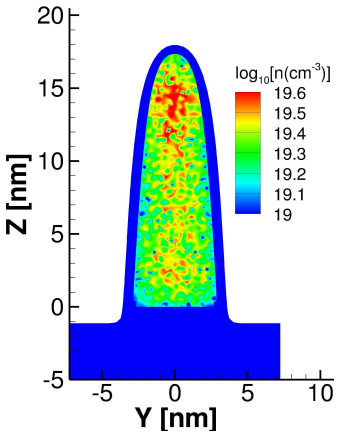

Fig. 6: Electron density in a cross-section through the middle of the gate in the wide-triangular ⟨100⟩ channel FinFET at V_G-V_T = 0.7 V, V_D = 0.7 V.

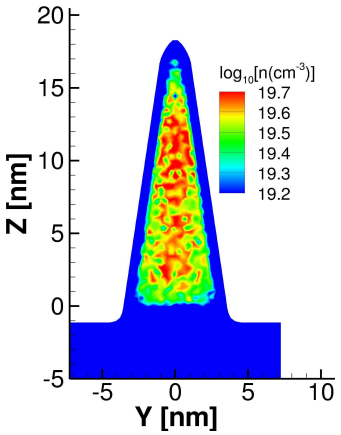

Fig. 7: Electron density in a cross-section through the middle of the gate in the narrow-triangular ⟨100⟩ channel FinFET at V_G-V_T = 0.7 V, V_D = 0.7 V.