Impact of Scaling on the Variability in Multigate Transistors

M. Aldegunde, A. Martinez, and J. R. Barker*
College of Engineering, Swansea University, Swansea SA2 8PP, United Kingdom
e-mail: m.a.aldegunderodriguez@swansea.ac.uk
*School of Engineering, Glasgow University, Glasgow G12 8LT, United Kingdom

Three-dimensional device architectures are strong candidates for the scaling of MOSFETs into the next technology nodes [1]. Two of the most important sources of fluctuations in ultrascaled devices are *random discrete doping* and *surface roughness*. Previous studies of variability have been concentrated in generic nanowire structures or used semiclassical models. In this work we study the impact of scaling on the effect of both sources of variability in two Si multigate MOSFETs scaled according to the ITRS.

We carried out non-equilibrium Green's functions (NEGF) transport simulations including all relevant phonon scatterings [2]. We study two different devices with channel lengths of 11.8 and 6.6 nm and body thicknesses of 5.8 and 4.2 nm, respectively. In both cases the ratio between the body height and thickness is 2:1. Random discrete doping (RDD) and surface roughness (SR) are introduced using the same methodology and the same parameters as in [3]. We have simulated five different configurations for each device, which should provide an estimation for the range of variability expected in a larger ensemble. Figs. 1 and 2 show the $I_D - V_G$ characteristics at a high drain bias V_D=700 mV for both simulated transistors under the combined influence of RDD and SR. The characteristics with a smooth geometry and doping are shown as a reference. For both geometries we see a shift towards higher threshold voltages due to a change in the width and height of the barrier induced by the different variability sources. This shift is smaller for the larger device, where it ranges from 6 to 22 mV, than for the shorter one, where it ranges from 20 to 77 mV. The main effect of the RDD in the low gate bias region is a change in the subthreshold slope. The variability is much larger in the case of the shorter device, where the slopes vary between 84 and 101 mV/dec, whereas in the longer device they vary between 76 and 81 mV/dec. Fig. 3 presents the local density of states and the subbands for the smooth device and the highest current configuration in the shorter device at V_G=0.6 V. The small amplitude ripples of the subbands close to source and drain reflect the SR while the large amplitude ones correspond to the RDD which are close to the source/channel and drain/channel interfaces. We can also see how the potential fluctuations induced by RDD and SR break the interference fringes in the LDOS seen in the smooth device. Fig. 4 shows the electron density and electrostatic potential energy for the highest current configuration of the 6.6 nm device at V_G=0.5 V. At the source cross-section, the electron density has two maximums due to the large electron electrostatic energy at the middle of the cross section. These two maximums merge in the middle of the source/channel interface cross-section due to the RDD concentration there. Finally, Figs. 5 and 6 show the spectral current density for the two geometries in the lowest and highest current configurations (V_G=0.3 V). For the longer device, there is a small difference in the barrier width and therefore in the tunnelling current. The main difference in the $I_D - V_G$ characteristics is a shift of about 16 mV, which comes mainly from the difference in barrier height (around 20 mV). For the shorter devices we can see a clear difference in the barrier width coming from RDD close to the channel, which reduce the effective gate length. This notably increases the tunnelling current and therefore the subthreshold slope. This increase is also strengthened by the lower height of the barrier induced by the SR (around 25 mV).

References

[1] T. Chiarella *et al.*, Solid-State Electron. **54**, 855 (2010).
[2] M. Aldegunde *et al.*, J. Appl. Phys. **110**, 094518 (2011).
[3] A. Martinez *et al.*, IEEE Trans. Electron Devices **58**, 2209 (2011).

978-3-901578-26-7

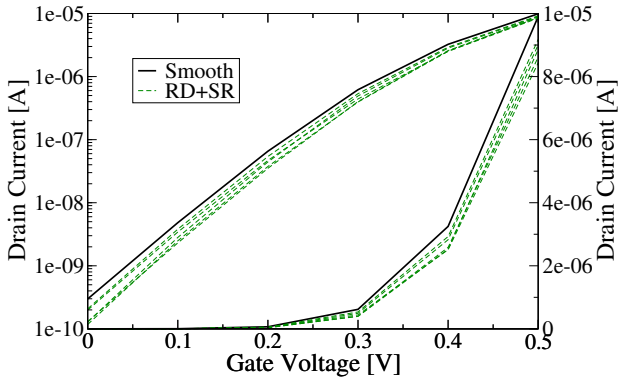

Fig. 1. $I_D - V_G$ characteristics of the 11.8 nm gate length MOSFET under the influence of discrete dopants and surface roughness. The smooth device (continuous black line) is also shown as a reference.

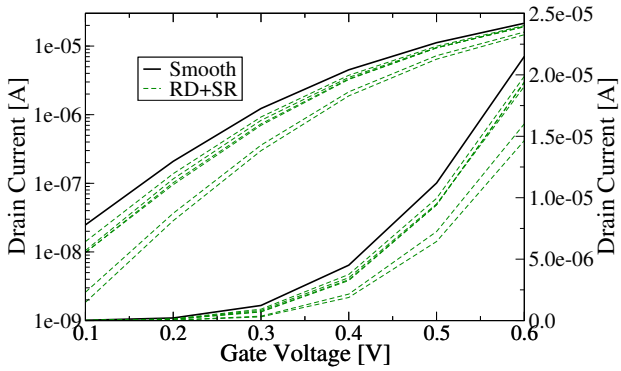

Fig. 2. $I_D - V_G$ characteristics of the 6.6 nm gate length MOSFET under the influence of discrete dopants and surface roughness. The smooth device (continuous black line) is also shown as a reference.

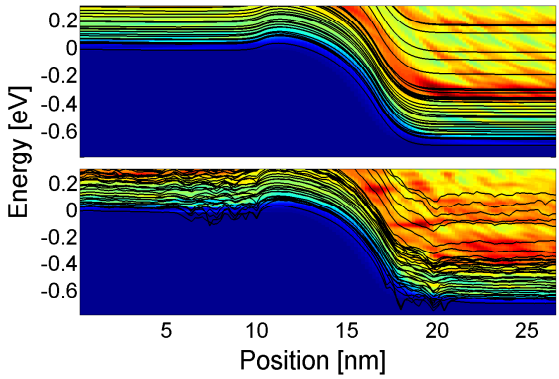

Fig. 3. Local density of states in the 6.6 nm gate length MOSFET for the smooth device (top) and under the influence of discrete dopants and surface roughness (bottom) at V_G=0.6 V.

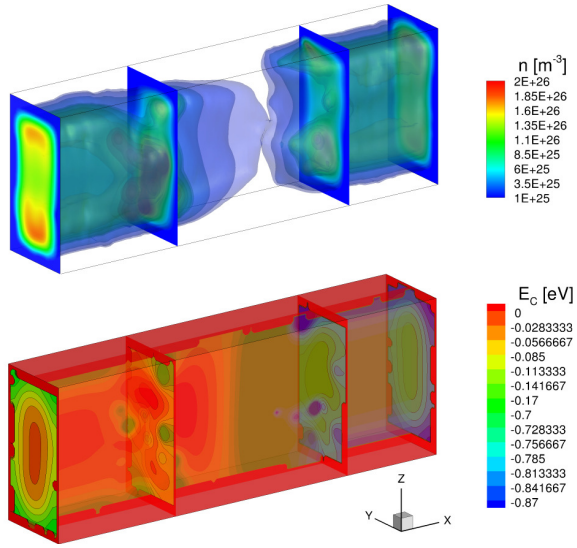

Fig. 4. Electron density (top) and electrostatic potential energy (bottom) for one random configuration of the 6.6 nm gate length MOSFET.

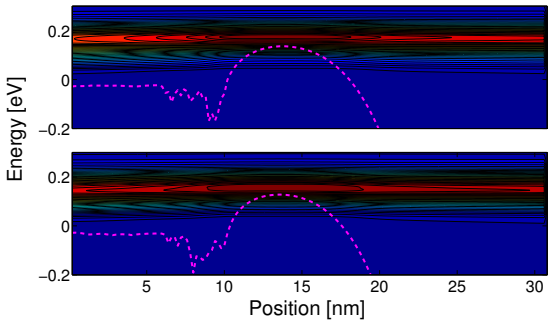

Fig. 5. Spectral current for the configurations with lowest (top) and highest (bottom) drain current for the 11.8 nm gate length MOSFET.

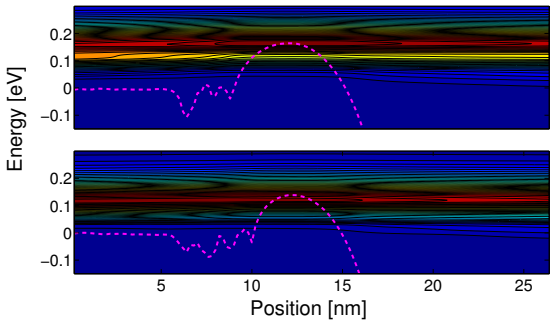

Fig. 6. Spectral current for the configurations with lowest (top) and highest (bottom) drain current for the 6.6 nm gate length MOSFET.