Intrinsic Region Length Dependence of Vertical Double Gate IMOS

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INTRODUCTION

CMOS technology has been scaling down in size following the Moore's law for over 40 years. As the size of the MOSFET is reduced rapidly into the nano scale region, they begin to suffer from a few critical issues. One of them is the increase of the subthreshold swing (S-Factor). Under ideal conditions, in which the gate oxide capacitance is infinite, S-Factor of the MOSFET becomes about 60 mV/dec at room temperature. As a result, short channel effect (SCE) brings the increase of S-Factor, the leakage current of the MOSFET increases substantially. At the same time, the threshold voltage (Vth) and supply voltage cannot be shrunken while keeping a sufficiently low off state current.

In order to solve the above problems, the I-MOS [1] is widely investigated as one of the promising approaches. In this paper, we investigated Vertical Double Gate IMOS (DGIMOS) as one of Multi-Gate type structures. The parameter dependences of Vertical DGIMOS are investigated. The variance of parameter characteristics of S-Factor, Vth and Ioff is analyzed with the decreasing of intrinsic region length (Li) of Vertical DGIMOS for the first time.

DEVICE STRUCTURE

Figure 1 and Table I show structure of vertical DGIMOS and the device parameters. Vertical DGIMOS structure is a kind of a gated p-i-n diode. Source/Drain doping concentration and p-type body concentration set to be 10^{20} cm^{-3} and 10^{17} cm^{-3} respectively. In the simulation, band-to-band tunnelling and impact ionization are considered.

RESULTS AND DISCUSSIONS

Figure 2 shows simulated I_{DRAIN} versus V_{GATE} characteristics of the Vertical DGIMOS under the condition that some of Li are 40, 34, 18 and 10 nm. Source voltage and Drain voltage are fixed -3V and 0V. In this paper, the definition of Vth is the gate voltage at which S-Factor is minimum, because S-Factor of vertical DGIMOS which is different from S-Factor of the MOSFET, isn't linear. Ioff is defined by the drain current when the gate voltage is zero. The S-Factor dependence of Li, the Vth dependence of Li, and the Ioff dependence of Li are given in Fig.3, Fig.4 and Fig.5 respectively. In the range that Li is set from 40 nm to 34 nm, S-Factor is improved with the reduction of Li and Vth becomes lower, Ioff becomes higher at the same time. In the range that Li is set from 34 nm to 18 nm, S-Factor is degenerated with the reduction of Li and Vth becomes lower, Ioff becomes higher at the same time. In the range that Li is set from 18 nm to 10 nm, S-Factor is degenerated with the reduction of Li and Vth becomes higher, Ioff becomes higher at the same time. As a result, the device simulation results clarify that parameter dependences of Li can be divided into 3 regions depend on impact ionization in intrinsic region and variance of channel potential.

CONCLUSION

The parameter dependences of Vertical DGIMOS are analyzed in detail in this paper. As important design guideline of DGIMOS, we found that parameter characteristics of S-Factor, Vth and Ioff show different behaviour in the three regions with the decreasing of Li.

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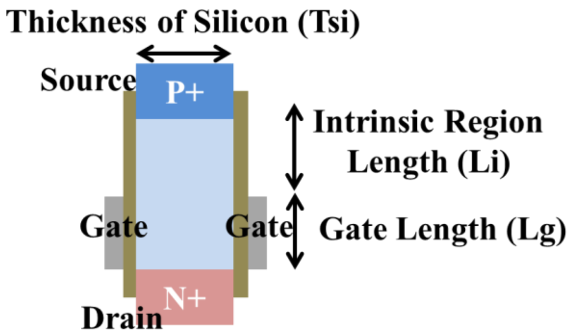

Fig. 1. Structure of the vertical double gate IMOS (DGIMOS).

Table I. Device parameters and values in Vertical DGIMOS

Device Parameter	Value
Intrinsic Region Length (Li)	10~40 nm
Gate Length (Lg)	40 nm
Gate Width (W)	1.0 μm
Thickness of Silicon (Tsi)	20 nm
Thickness of Oxide (Tox)	1.2 nm

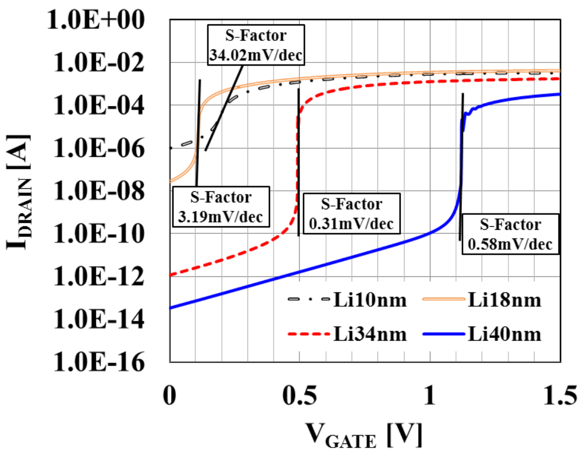

Fig. 2. Simulated I_{DRAIN} versus V_{GATE} characteristics of the vertical DGIMOS with V_D=0V and V_S=−3V.

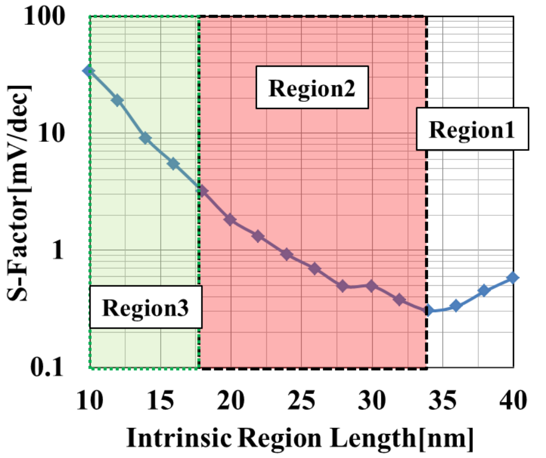

Fig. 3. The S-Factor dependence of Li in vertical DGIMOS.

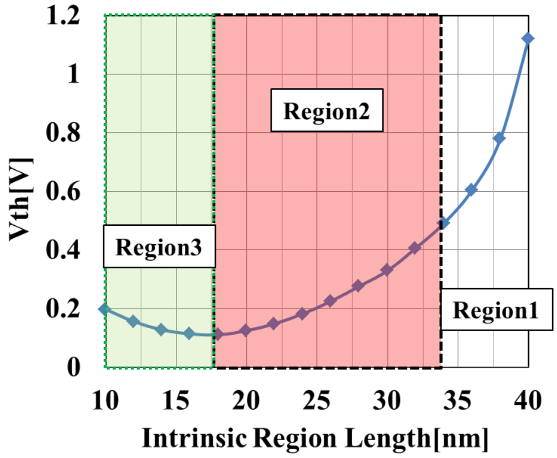

Fig. 4. The threshold voltage (Vth) dependence of Li in vertical DGIMOS.

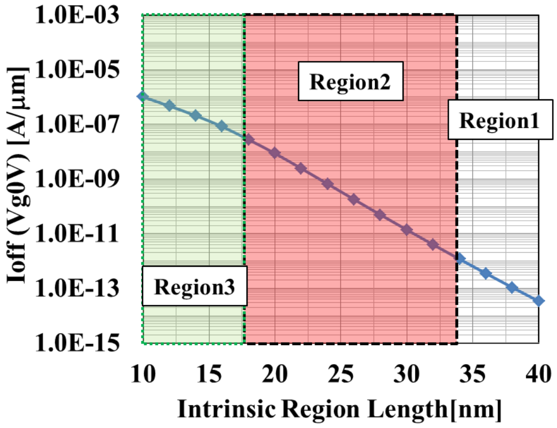

Fig. 5. The Ioff dependence of Li in vertical DGIMOS.