Gate Leakage Reduction of Vertical MOSFET with High-k Dielectric Film Employing Gate Dielectric Capacitance Oriented Design

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INTRODUCTION

Gate dielectric capacitance per unit area (C_{ox}) and equivalent oxide thickness (EOT) are one of the key design parameters of MOSFET to reduce gate leakage with high driving current in continuing scaling of the replacing gate dielectric material thermal silicon dioxide to high permittivity dielectrics. The Vertical MOSFET (VMOS) [1] has been intensively studied due to the strong gate controllability caused by its cylindrical silicon pillar and gate stack. This letter addresses the importance of the cylindrical structure of the VMOS and shows the significant gate leakage reduction by 99.2% with 1.67 times larger driving current in the case of the same C_{ox} of the Double Gate MOSFET (DG) at EOT=0.3nm.

GATE DIELECTRIC CAPACITANCE OF VERTICAL MOSFET WITH HIGH-K DIELECTRIC FILM

The C_{ox} of the VMOS ($C_{ox,VMOS}$) [1] as eq. (1),

$$C_{ox} = k \times \left[R \ln\left(1 + \frac{t_{ox}}{R} \right) \right]^{-1} \quad (1)$$

where R is the silicon pillar radius, t_{ox} is the gate dielectric thickness, and k is the dielectric constant of the gate dielectric materials. The ratio (α) of the $C_{ox,VMOS}$ to the C_{ox} of the DG ($C_{ox,DG}=k/t_{ox}$) is plotted versus k at the same EOT=0.3nm in Fig. 1(a). The EOT is defined by EOT=t_{ox}/(k/3.9). In the case of the same EOT, $C_{ox,VMOS}$ is the α times larger than $C_{ox,DG}$. Therefore, the t_{ox} of the VMOS is α times thicker than that of the DG at the same $C_{ox,VMOS}$ as the $C_{ox,DG}$ in Fig. 1(b).

INVESTIGATION OF THE GATE DIELECTRIC CAPACITANCE ORIENTED DESIGN

The gate leakage and driving current performances of the VMOS is investigated through Sentaurus device simulator [2]. Figure 2 shows the simulated device structures and Table I shows the device parameter settings. In the case that the $C_{ox,VMOS}$ is the same as the $C_{ox,DG}$, the gate leakage current density of the VMOS is reduced by 99.2% applied at the high gate voltage (V_{gate}–V_{th}=0.340V) in the comparison with the DG due to the α times thicker (0.56nm) t_{ox} than that of the DG in Fig. 3. The driving current normalized by channel width of the VMOS is increased by 1.67 times than that of the DG in Fig. 4. The increase of the driving current in the VMOS is caused by high electron density in the channel region in Fig. 5. The VMOS obtains higher electron density by 3.1 times than that of the DG at the silicon pillar center in Fig. 6. Therefore, the C_{ox} oriented design in the VMOS with high-k gate dielectric can obtain the reduction of the gate leakage with high driving current.

CONCLUSION

The gate leakage and driving current performances of the VMOS with high-k dielectric film is investigated in the comparison with the DG at the EOT=0.3nm. The VMOS reduces the gate leakage by 99.2% due to its cylindrical nature. The results are fruitful for the future high performance and low gate leakage device design with ultra-thin higher-k gate dielectrics.

ACKNOWLEDGEMENT

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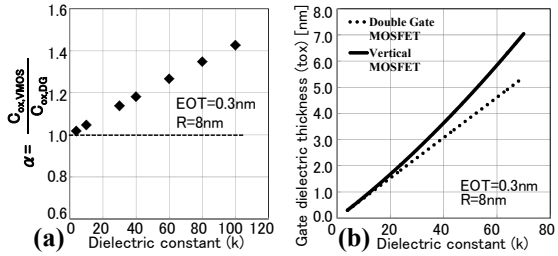

Fig. 1. (a) The ratio (α) of the C_{ox} of the VMOS to that of the DG versus k at the same EOT=0.3nm. (b) The α times thicker t_{ox} of the VMOS than that of the DG at the same C_{ox} in the EOT=0.3nm.

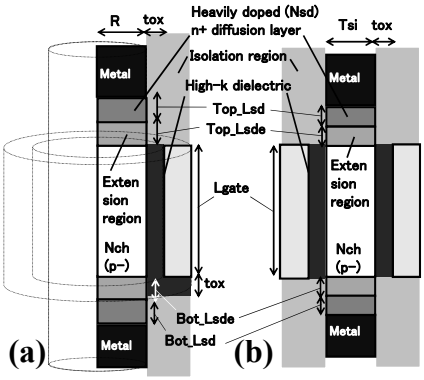

Fig. 2. Simulated device structures. (a) Vertical MOSFET, (b) Double Gate MOSFET. The VMOS and the DG was numerically solved in cylindrical coordinates and in two-dimensional simulation, respectively.

Table I. Device parameter settings.

Device parameters	VMOS	DG
Silicon pillar diameter (2R)	16nm	
Silicon thickness (Tsi)		16nm
Gate length (Lgate)	24nm	
Gate dielectric thickness (tox)	0.3～3.64nm	
Gate dielectric constant (k)	3.9～40	
Gate workfunction	4.4eV	4.6eV
Channel concentration (Nch)	1e17cm^{-3}	

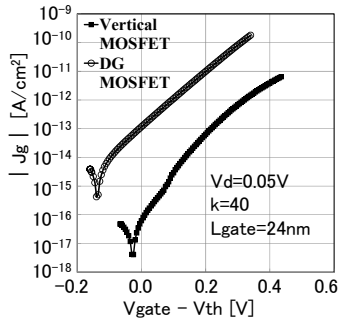

Fig. 3. Reduction of the gate leakage current density of the VMOS in the comparison with the DG in the case of the same C_{ox}. The V_{th} in Fig. 3 is extracted by constant-current method at I_d/(channel width)=100nA/μm in the linear region (V_d=0.05V).

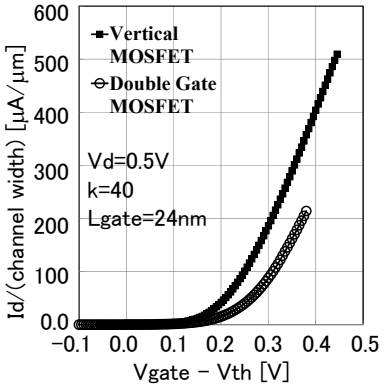

Fig. 4. Driving current normalized by channel width characteristic of the VMOS and the DG in the case of the same C_{ox}. The V_{th} in Fig. 4 is extracted by constant-current method at I_d/(channel width)=100nA/μm in the saturation region (V_d=0.5V).

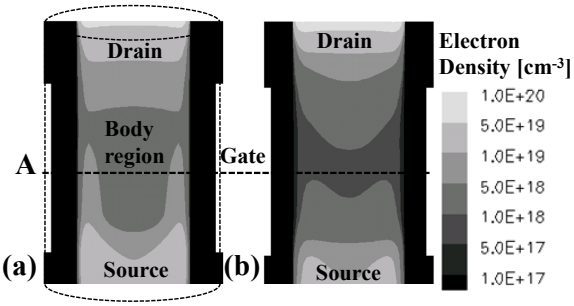

Fig. 5. Electron density distribution in the channel (a) VMOS and (b) DG at the V_{gate}-V_{th} =0.380V in the saturation region (V_d =0.5V). Even if the thicker t_{ox} than α times that of the DG, the electron density in the body region is larger than that of the DG, which leads to high driving current of the VMOS.

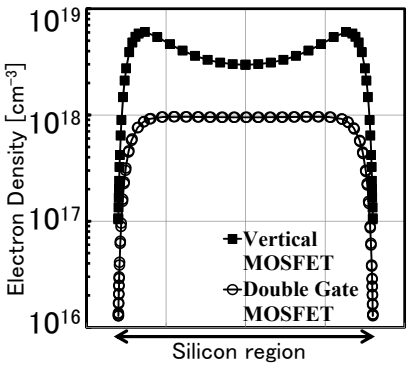

Fig. 6. High electron density of the VMOS in the body region at the dashed line A in Fig. 5.