On Rounding and Taper Fins of FinFET Varactors

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I. INTRODUCTION

Bulk FinFET is one of the candidates for device in sub-22 nm technology node, because of its good cut-off characteristics, short channel effect control and better scalability by miltiple gate mode operation [1-3]. Recent studies on FinFET devices were reported (see, for examples, [4-7], and references therein), but the influence of fin profile on device's capacitance has not yet clearly been investigated.

In this work, we experimentally fabricate and characterize HKMG bulk FinFET devices and simulated the fin profile with different tapers and rounding. The influence of the fin taper and rounding profile on C-V characterization is assessed, where the fabrication parameters are extracted accordingly.

II. EXPERIMENT AND SIMULATION

The devices we studied are the HKMG bulk FinFETs on (100) p-substrate, where the C-V curves are measured as shown in Fig. 1. To fabricate the devices, the advanced 193 nm immersion lithography and optimized etching processes are then utilized for silicon fin and STI formation. Then, a 1.5-nm-thick chemical oxide and a 3-nm-thick HfO_3 film are deposited by chemical vapor deposition. Finally, we use sputter to form 12-nm-thick TiN film, as shown in Fig. 2. Fig. 2 further indicates the profile of fin with taper and rounding due to the fabricated etching process.

Fig. 3 shows that 3D computational device model, where a set of quantum-mechanically transport equations is solved to calculate the device's characteristic. Notably, the right plots are the model cross section views of the fin profiles which are with respect to different taper and rounding. The taper varies from 0, 1, 3, and 5 degrees and the radius is from 1, 3, 6, 7, and 8 nm.

III. RESULTS AND DISCUSSION

As shown in Fig. 4, the simulated device's capacitance with different taper profiles, where the Radius = 0 and the Taper = 0, 1, 3 and 5. The capacitances are 8.20, 8.10, 7.78 and 7.55 fF, respectively at accumulation region. Their C_{min} are 2.31, 1.60, 1.32 and 1.25 fF, respectively. When the fin profile is more taper, the device is with smaller capacitance. As shown in Fig. 5, the simulated capacitance with different rounding profile devices (Taper = 0, Radius = 1, 3, 5, 7 and 8 nm) are 8.20, 8.03, 7.73, 7.48 and 7.37 fF, respectively, at accumulation region. Also, their C_{min} are 2.31, 2.18, 2.38, 1.63 and 1.61 fF, respectively. When the fin profile is with a larger taper, the device will be with a relatively smaller capacitance.

From the C-V curves simulated, we can extract the parameter of fin profile by fitting the measured C-V curves. As shown Fig. 6, the matching between the simulation and characterization is well. The extracted taper of the fabricated HKMG bulk FinFET sample is 5 deg. and the rounding radius is 8 nm. The extracted taper angle and the rounding radius owing to process variation effect can be modeled into device model for variability simulation of FinFET circuits.

IV. CONCLUSIONS

The 3D device simulation of FinFET varator devices with different taper and rounding profile has been demonstrated. The findings of this study have been calibrated with the silicon data by matching the measured capacitance, where the fabrication parameters haven been extracted.

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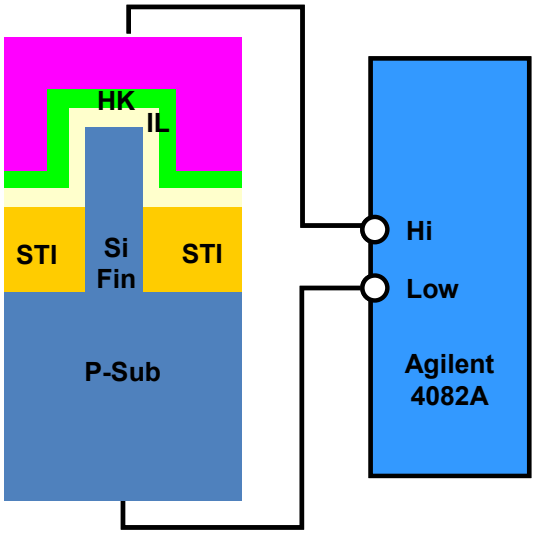

Fig. 1. Cross-section view of the fin MOSCAP and the measurement configuration of C-V curves, we measure the device's C-V curves by the 4082A Parametric Test System.

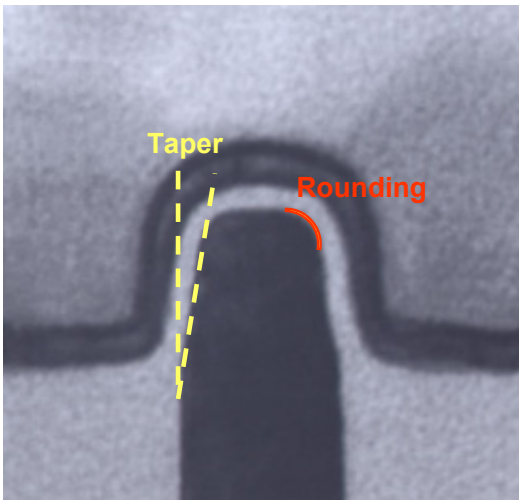

Fig. 2. The TEM of the fabricated Fin-type varator with a 20-nm fin width. Notably, the taper and rounding fin profiles are obviously.

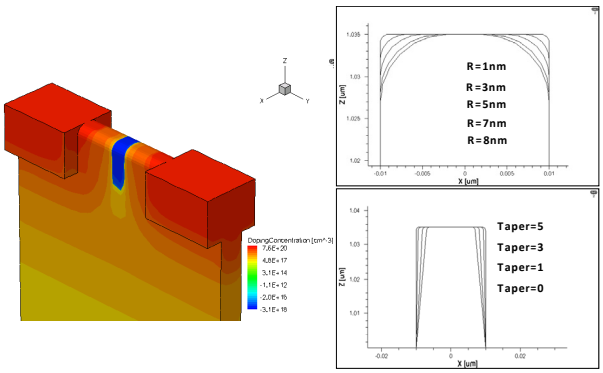

Fig. 3. The 3D simulation structure; the left plot is a 3D fin, and the right lots are the cross sections of the model with different angles of taper (θ = 0, 1, 3, and 5 deg.) and the rounding radius = 1, 3, 5, 7, and 8 nm.

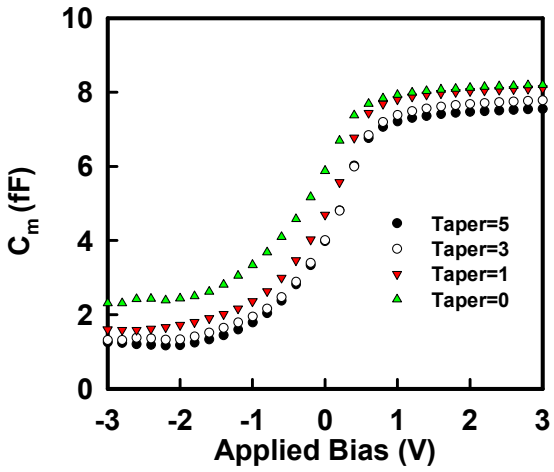

Fig. 4. The simulated C-V with different taper profile devices. When the fin profile is with a larger taper, the device is with a smaller C_{min} at the accumulation region.

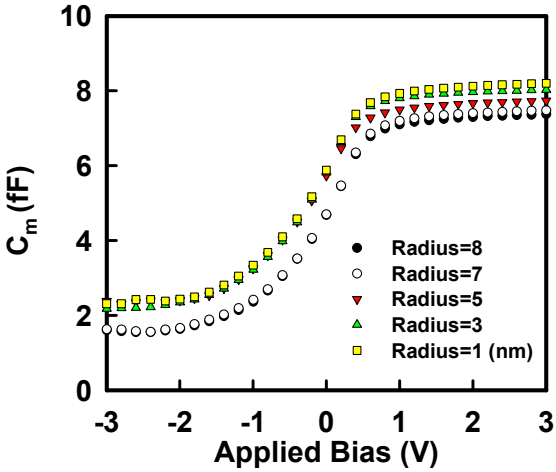

Fig. 5. The simulated C-V with different rounding profile devices. When the fin profile is with a larger rounding, the device is with a smaller C_{min} at the accumulation region.

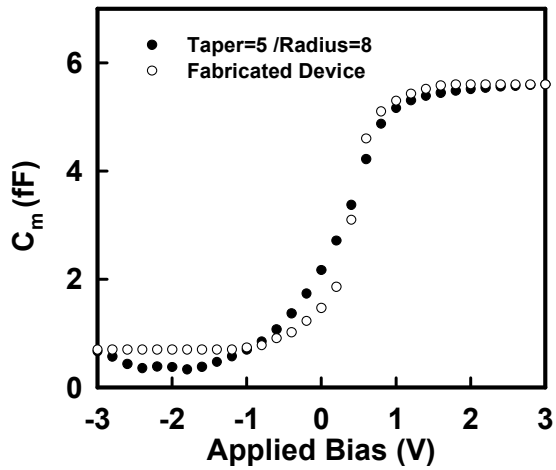

Fig. 6. The simulated and the measurement capacitances. The matching of the C-V curves is validated for the sample with the extracted taper and rounding.