Effect of Fin Tapering in Nanoscale Si FinFETs

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INTRODUCTION

For the past 40 years scaling has enabled a sustained improvement in the transistor performance while increasing transistor density. The historically planar MOSFET has evolved into a 3D FinFET at the 22nm node to mitigate short channel effects [1, 2].The TEM images reveal that the 'fin' deviates from a popularly assumed rectangular shape to a tapered sidewall structure attributed to the process conditions used for fabrication [1, 2]. Such loss of control on the final shape of the FinFET may lead to unwanted variations in MOSFET performance. The present paper investigates the impact of fin tapering, in nanoscale FinFETs, on its DC performance using atomistic simulations in the ballistic limit.

DEVICE SIMULATION APPROACH

The effect of tapering is studied in unstrained, Si FinFETs with <110> channel orientation fabricated on a (100) wafer (Fig.1). The fin height is fixed at 10 nm while the base width is set to 6 nm. The effect of sidewall slanting is taken into account by introducing a taper angle, θ (Fig. 1). An effective oxide thickness of 1.2 nm as assumed (Fig. 1). Id-Vg characteristics are simulated using the 'Top-of-the-Barrier' transport model solved in a self consistent fashion (Fig. 2) [3, 4]. To capture the quantum effects accurately 10 band $sp^3d^5s^*$ (including SO-coupling for valence bands) tight binding (TB) model is employed for solving the Schrodinger equation [5]. A zero electric field (Neumann) boundary condition is used at the base of the Fin for the Poisson solution. The ON state is defined as the drain current (I_{DS}) atV_{GS}=V_{DS}=0.7V, with the fixed OFF state at I_{DS}=100nA/µm. Current values are normalized by the base width (=6nm).

RESULTS

Fig. 3 shows the Id-Vgplots for n/p- FinFETs with different W_{TOP}. Interestingly, p-FinFETs exhibit negligible variation in current, unlike n-FinFETs.This phenomenon is well explained by the interplay between the ON state charge (N_{inv}) and carrier injection velocity (v_{inj}). Holes show a preferential movement towards the (110) sidewalls (Fig. 4b) whereas electrons prefer reside near the (100) top-gate (Fig. 4a) [6]. Since the (110) side gates are much longer than the (100) top-gate, it leads to higher inversion charge in p-FinFETs compared to n-FinFETs at the ON state (Fig. 5a). Tapering of the fin reduces the perimeter where the gate acts leading to a reduction in the effective gate to channel capacitance thus, reducing the N_{inv} for both n and p-type FinFETs. With fin tapering the electron v_{inj} is not modulated much however, for holes,v_{inj} increases with fin tapering (Fig. 5). This nearly cancels the degradation in charge leading to negligible effect on the p-FinFET ON-current. v_{inj} is almost unaffected with tapering in n-FinFET which ultimately causes the final ON state current to degrade by nearly 30% as taper angle reduces from 90 to 77.3 degrees.

CONCLUSION

FinFET tapering severely degrades the ballistic ON current in n-FinFETs (coefficient of variation =15%) with negligible change in p-FinFETs (coefficient of variation =2%).

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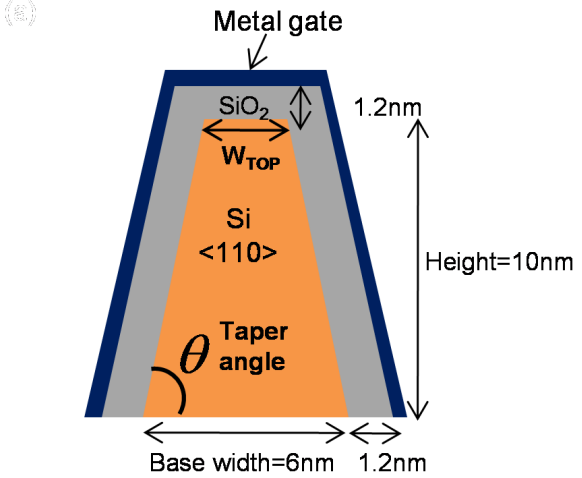

Fig. 1 Si FinFET structure considered in this study.

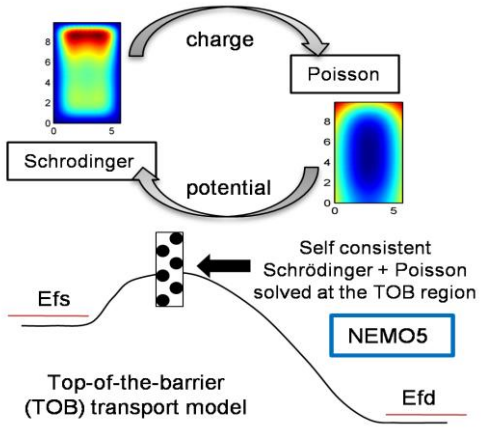

Fig. 2. Schematic description of the semi-classical top of the barrier transport model.

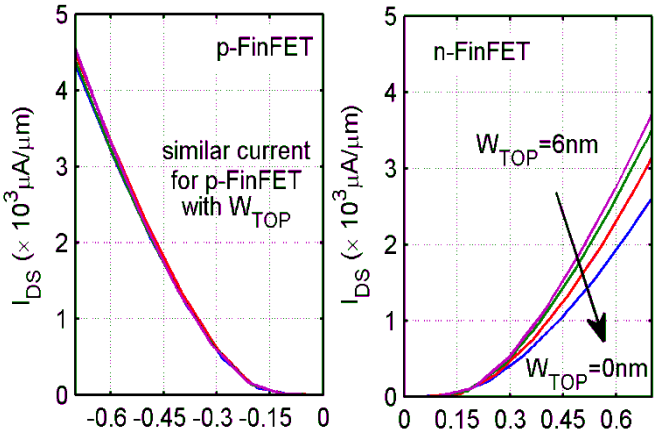

Fig. 3. . Ballistic Id-Vg plots for n-type and p-type Si FinFETs. Current values are normalized by the base width (=6nm)

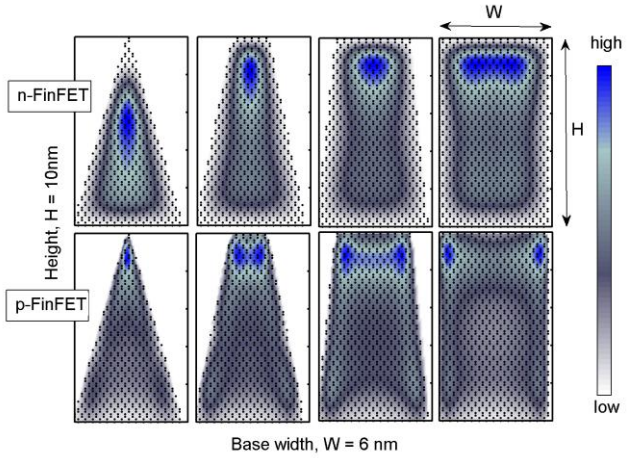

Fig. 4. Normalized charge distribution in (a) n-type (top row) and, (b) p-type (bottom row) Si FinFETs at the ON state (Vgs=Vds=0.7V).

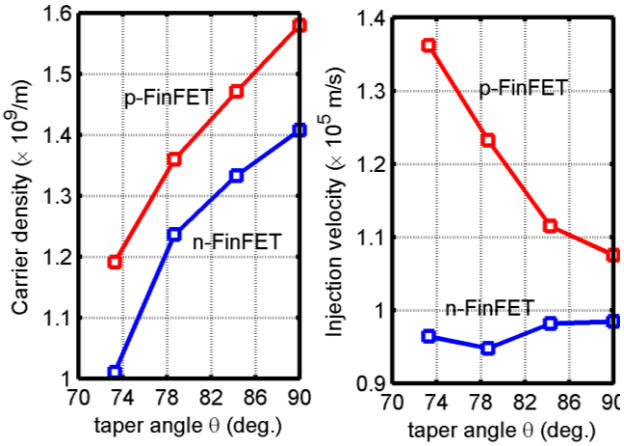

Fig. 5. ON state carrier density (left) and injection velocity (right) for n-type and p-type Si FinFETs.

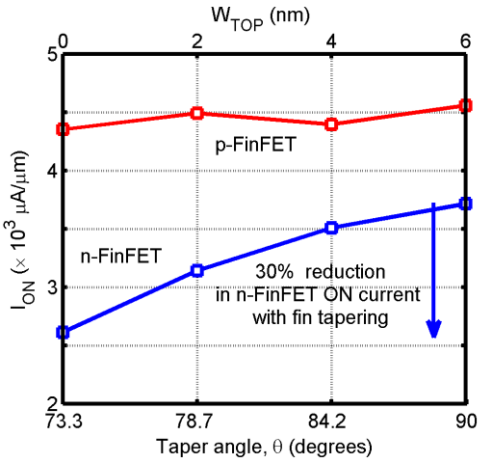

Fig. 6. Variation in ballistic ON current with taper angle (or W_{TOP}).