SNM Improvement for SRAMs Composed of High Mobility Channel MOSFETs

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With an increase in demand for high speed and/or low power operation of CMOS devices, high mobility channel MOSFETs, such as Ge- and $In_xGa_{1-x}As$ MOSFETs, for instance, are being intensively investigated. Comparing these MOSFETs with Si ones under a condition of the same operation speed, the cutoff characteristics are expected to be improved because $|V_{TH}|$ can be set higher than the Si ones. Therefore, SNM of SRAMs with the high-mobility MOSFETs is also expected to be improved. In this paper, 6T-SRAM cells composed of MOSFETs having a Si-, Ge-, and $In_{0.53}Ga_{0.47}As$ channel are comparatively studied from a viewpoint of SNM and power consumption using device and circuit simulations.

Current-voltage characteristics for planar MOSFETs with a semiconductor-on-insulator structure were calculated using a device simulator HyENEXSS™ [1]. Device parameters are summarized in Table I. Figure 1 shows calculated relationships between the off-state current, I_{OFF}, and the effective drive current, I_{eff} [2], at a given operation voltage, V_{DD}. Here, I_{eff} was introduced as an index of the operation speed. The result shows that I_{OFF} for the Ge- and the $In_{0.53}Ga_{0.47}As$ FETs are lower than the corresponding values for the Si FETs at a fixed I_{eff}. This is because $|V_{TH}|$ was set higher for the high-mobility FETs. In the following calculation, parameters for the Ge- and the $In_{0.53}Ga_{0.47}As$ FETs were adjusted so that their I_{eff} matched to the value for the Si FETs with I_{OFF} = 100 nA/μm. Voltage transfer characteristics were calculated for Si-, Ge-, and Hybrid ($In_{0.53}Ga_{0.47}As$ nFET/Ge pFET) inverters using a circuit simulator SmartSpice [3] (Fig. 2). The reason for the steep switching of the Ge- and the Hybrid inverters is the lower I_{OFF} of FETs in these inverters than that of FETs in the Si inverter (Fig. 1). Butterfly curves of Si-, Ge-, and Hybrid SRAMs were calculated (Fig. 3). SNM of the Si/Ge/Hybrid SRAMs was calculated to 0.14/0.18/0.19 V. The reason for the large SNM of the Ge- and the Hybrid SRAMs is the steeper switching of the Ge- and the Hybrid inverters than that of the Si inverter.

In order to study influences of V_{TH} variation on SNM, V_{TH} of 6 FETs in the SRAM were shifted independently by an amount of ΔV_{TH}. SNM with V_{TH} variation was defined by a minimum SNM of the 2^6 = 64 cases (Fig. 4). Qualitatively equivalent results were obtained for V_{DD} of 1.0, 0.8, 0.6, and 0.4 V. Even in the case that V_{TH} variation is taken into consideration, SNM of the Ge- and the Hybrid SRAMs is larger than that of the Si SRAM. Extrapolating the relationships between ΔV_{TH} and SNM in Fig. 4, ΔV_{TH} at which SNM = 0 V was calculated, which is considered to be a maximum permissible V_{TH} variation in the SRAM (Fig. 5). Using a reported value of 25 mV as a standard deviation of V_{TH} (σV_{TH}) [4] and assuming that ΔV_{TH} = 3 x σV_{TH} = 75 mV, lowest V_{DD} values of the Si/Ge/Hybrid SRAMs were calculated to be 0.93/0.72/0.63 V. Standby power ($\propto I_{OFF}$ x V_{DD}) of the Ge/Hybrid SRAMs was estimated to be 1.1/0.39% of the Si SRAM due to the lower I_{OFF}.

In conclusion, high mobility channel MOSFETs are effective for SRAMs in SNM improvement, resulting in standby power reduction.

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[3] http://www.silvaco.com/products/circuit_simulation/smartspice.html
[4] Z. Ren, et al., *Assessment of Fully-Depleted Planar CMOS for Low Power Complex Circuit Operation*, IEDM Tech. Dig., 366 (2011)

Table I. Device parameters.

Gate Length	25 nm
Thickness:	
Channel Layer	10 nm
Buried Insulator	20 nm (SiO_2)
Gate Insulator	1 nm (SiO_2)
Gate Sidewall	20 nm (Si_3N_4)
Handle Wafer	100 nm (Si)
Impurity Concentration:	
Channel Region	1 x 10^{15} cm^{-3}
Handle Wafer	1 x 10^{18} cm^{-3}
Source and Drain Regions:	
Peak Impurity Concentration	3 x 10^{20} cm^{-3}
Offset Spacer Thickness	0 to 20 nm
(Varied in order to adjust I_{OFF})	
Channels: [110] direction in (001) surface, unstrained.	

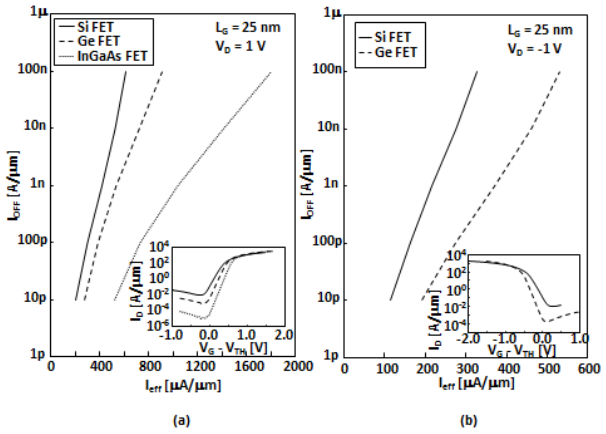

Fig. 1. Relationships between I_{OFF} and I_{eff} (= {$I_D(|V_G| = V_{DD}, |V_D| = V_{DD}/2) + I_D(|V_G| = V_{DD}/2, |V_D| = V_{DD})$}/2) [2] for (a) nFETs and (b) pFETs. Insets show I_D-V_G characteristics; I_{eff} are set equal to that of the Si FETs with I_{OFF} = 100 nA/μm.

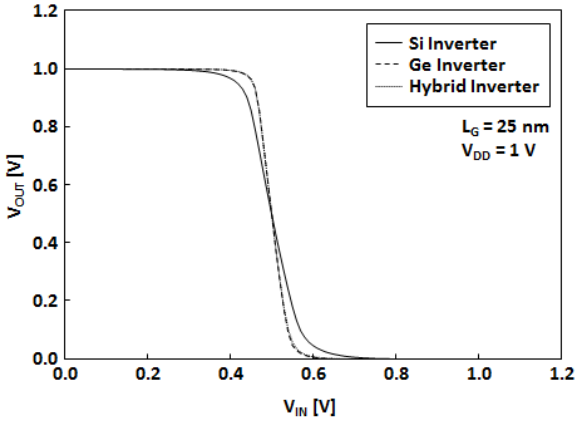

Fig. 2. Voltage transfer characteristics of Si-, Ge-, and Hybrid inverters.

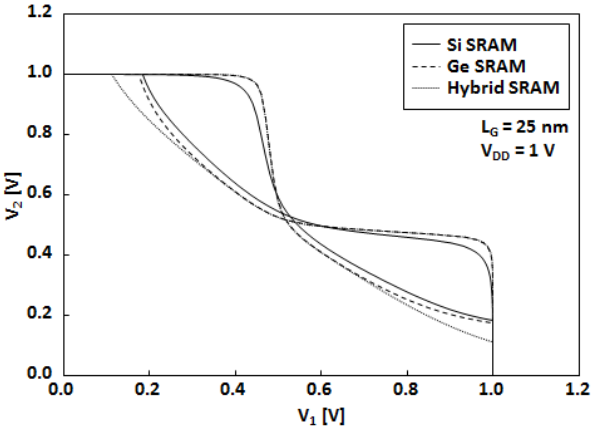

Fig. 3. Butterfly curves of Si-, Ge-, and Hybrid SRAMs.

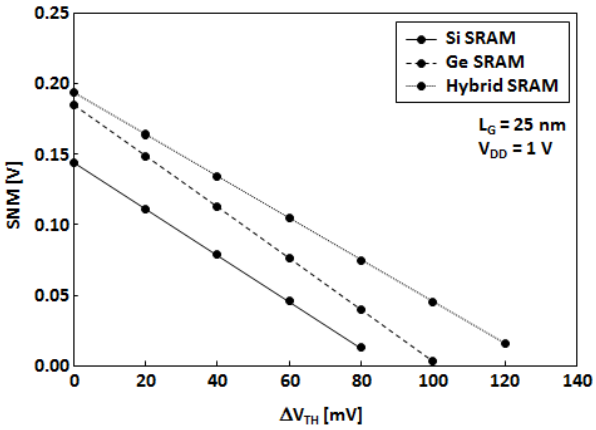

Fig. 4. Dependences of SNM on amount of V_{TH} variation (ΔV_{TH}) for the Si-, the Ge-, and the Hybrid SRAMs.

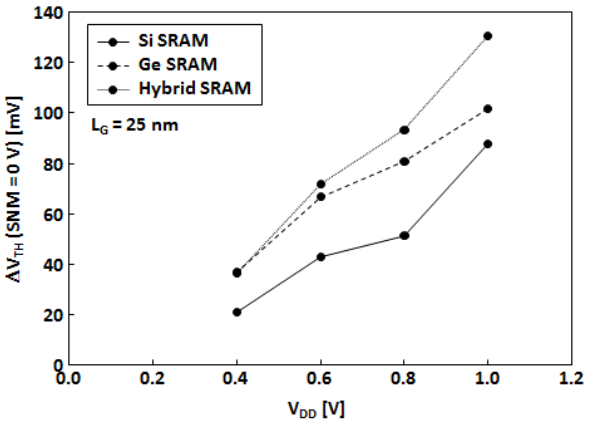

Fig. 5. Dependences of amount of V_{TH} variation (ΔV_{TH}) at which SNM = 0 V on V_{DD} for the Si-, the Ge-, and the Hybrid SRAMs.