Mixed-mode Simulation of Reconfigurable Si Nanowire Schottky Barrier Transistors Based Circuits

Juncheng Wang, Gang Du*, Kangliang Wei, Lang Zeng, Xiaoyan Liu *
Institute of Microelectronics, Peking University, Beijing, 100871, China
*e-mail: gangdu@pku.edu.cn, xyliu@ime.pku.edu.cn

INTRODUCTION

The reconfigurable Si nanowire Schottky barrier transistors (RFETs) are presented recently which show the variable electric characteristics and high on/off current ratio [1-3]. In contrast to conventional Schottky barrier Si nanowire transistors (SB-Si-NWTs) with metal/silicide as source/drain, the separate two gates in RFETs are located at the two Schottky junctions. Here we focus on the performance of RFETs base circuit. Some important parameters such as gate capacitance and cut-off frequency, which determine the behavior of RFETs in the analog/digital circuits are studied and compared with conventional SB-Si-NWTs.

The mixed-mode circuit simulation has been done for RFETs Inverter. Results of these simulations can give insights into the in-circuit behavior of these future generation devices.

SIMULATION METHOD AND DEVICE STRUCTURE

In our work, the performance of SB-Si-NWTs and RFETs is simulated with 3D device simulator Synopsys Sentaurus TCAD tool. The small-signal AC simulation and mixed-mode circuit simulation are carried out with it. We have considered drift diffusion transport within the Si region, thermionic emission and quantum mechanical tunneling at the Schottky junctions [4].

The schematic structures of the SB-Si-NWTs and RFETs for the simulations are plotted in Figure 1(a, b), with parameters given in Table Ⅰ. The circuit of RFET Inverter for mixed-mode circuit simulation is shown in Figure 1(c). Compared with conventional SB-Si-NWTs with metal/silicide as source/drain, the separate two gates in RFETs are located at the two Schottky junctions: program gate (Vg2) is to select p-/n-type configuration, control gate (Vg1) is to control the injection of the desired carriers into the channel. Intrinsic SB-Si-NWTs are used in our simulations. The silicide Schottky barrier height (SBH) is chosen to be 0.9 eV (such as PtSi) and 0.66eV (such as $NiSi_2$, the Fermi level of which aligns near the intrinsic Fermi level of Si [1]).

RESULTS AND DISCUSSION

The transfer curves of SB-Si-NWT and RFETs when SBH=0.9 eV and 0.66 eV are simulated in Fig. 2 (a), (b). Fig. 2 (a) shows that the Schottky Barrier transistors suffer from their ambipolar nature which leads to lower on/off current ratio about 1×10^5 when Vds= − 0.8V. The Drain Source voltage bias has much effect on the SB-Si-NWT, resulting in a shift of minimum drain-source current and lower on/off current ratio. Fig. 2 (b) plotted the transfer curves of RFETs when SBH=0.66eV. Due to the separated two gates in RFETs located at the two Schottky junctions, the RFETs can achieve much lower off-state current and higher on/off current ratio about 1×10^{15}. Besides, the Drain Source voltage bias has little influence on the RFETs compared with SB-Si-NWT.

The gate capacitance Cg of pSB-Si-NWT and p-type RFET as a function of gate voltage bias under different frequencies are shown in Fig. 3(a), (b). Cg of SB-Si-NWT and RFETs both decrease with the increasing frequency. For the ambipolar nature, Cg vs. gate voltage characteristic of pSB-Si-NWTs is almost symmetrical. However, when gate voltage changes from the negative to the positive, RFET is from on-state to off-state, and RFET decreases more slowly when on-state because it is easier for the inversion layer to form in the surface. Fig. 4 shows the high-frequency performances of SB-Si-NWT and RFETs.

To give insights into the circuit behavior of RFETs, we have carried out the mixed-mode circuit simulation for RFETs inverter. Fig. 5 shows us the voltage transfer characteristic of RFETs inverter when Vdd=1, 1.2, 1.5V. Transient analysis of RFETs inverter with a load capacitance of 0.05 fF is plotted in Fig. 6. The results show the delay of about 75ps and the inverter overshoot of about 10% Vdd in RFETs inverter.

CONCLUSION

The device characteristics and mixed-mode circuit behavior of RFETs are investigated through simulation. Gate capacitance and cut-off frequency of RFETs are studied and compared with SB-Si-NWTs. Our simulation results show the variable electric characteristics and higher on/off current ratio of the RFETs. Transient analysis shows the delay of about 75ps and the inverter overshoot of 10% Vdd in RFETs inverter.

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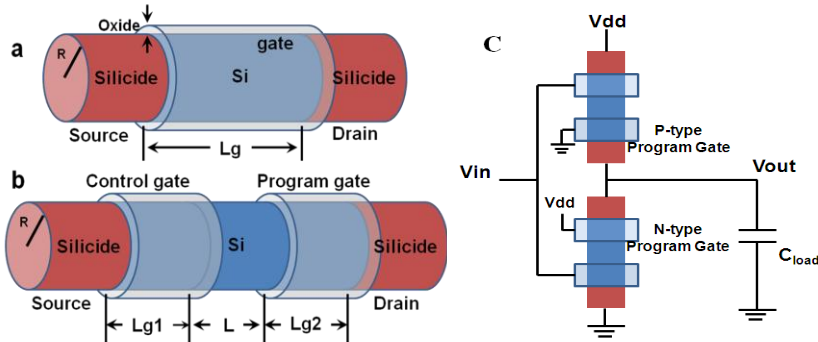

Fig. 1 The schematic structures of (a) SB-Si-NWTs and (b) RFETs for the simulations; (c) Circuit of RFET Inverter for mixed-mode circuit simulation.

TABLE I DEVICE PARAMETERS

PARAMETERS	VALUE
Gate Length (Lg/Lg1/Lg2)	30 nm
Length Between Two Gates (L)	30 nm
EOT(Tox)	1 nm
NWT Radius (R)	8 nm
Silicide Schottky barrier height (SBH)	0.9 eV, 0.66eV

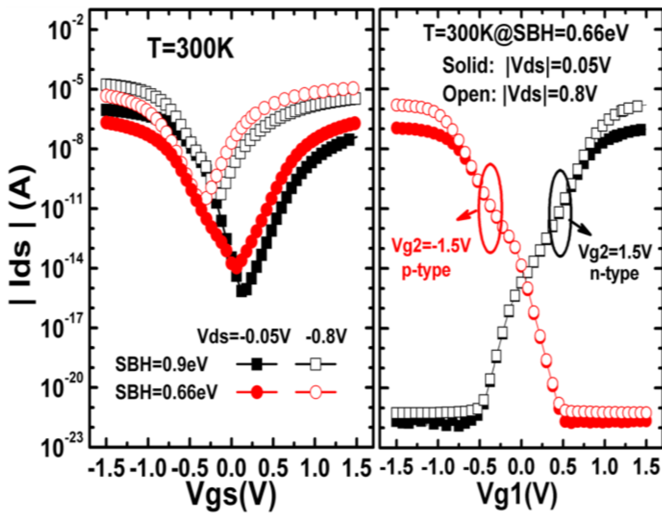

Fig. 2 The transfer curves of (a) SB-Si-NWTs and (b) RFETs.

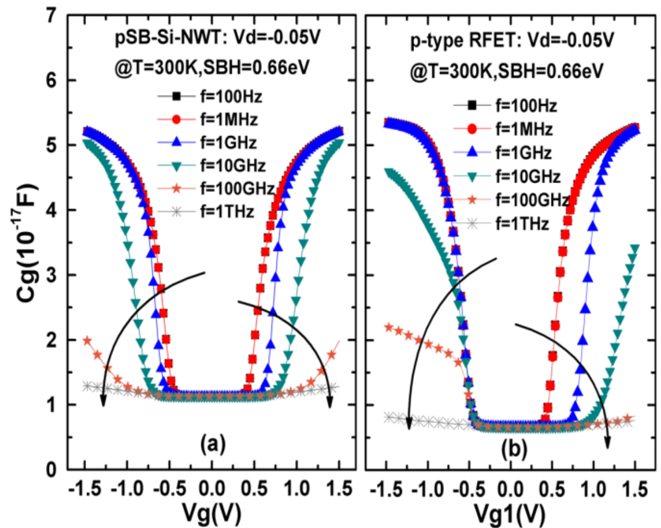

Fig. 3 Gate Capacitance vs. gate voltage characteristics of (a) pSB-Si-NWT and (b) p-type RFET when SBH=0.66eV under different frequencies.

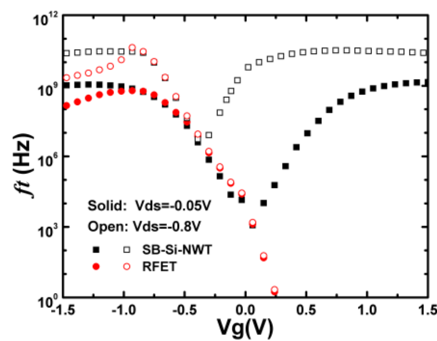

Fig. 4 The Cut-off frequency f_T vs. gate voltage characteristics of pSB-Si-NWT and (b) p-type RFET.

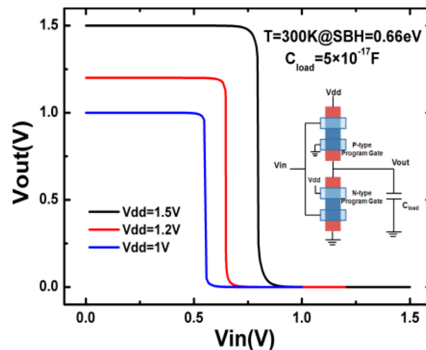

Fig. 5 Voltage transfer characteristic of RFETs inverter

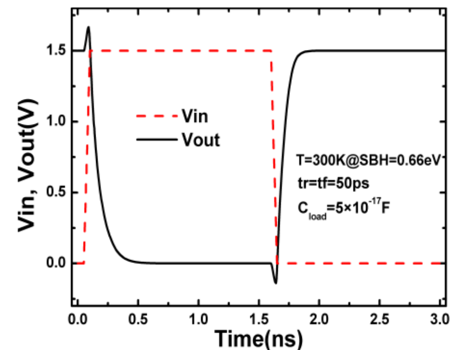

Fig. 6 Transient analysis of RFETs inverter