

Device Simulation of Hall Effect around Grain Boundaries in Poly-Si Films

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INTRODUCTION

Device simulation has been recognized as a powerful tool to develop and design semiconductor devices. However, few simulation algorithms have been published to calculate carrier transport subject to Lorentz force due to magnetic field. On the other hand, Hall effect arising from the Lorentz force have been utilized to evaluate material properties and diagnose fabrication processes. Recently, it was found that the evaluation technique using the Hall effect can be utilized also for poly-Si films [1]. Moreover, it was proposed that the micro poly-Si Hall cells can be applied to high-resolutional real-time magnetic sensors [2]. However, complicated Hall effect may occur because of uneven structures in poly-Si films, and no detailed discussion has been executed for carrier transport subject to the Lorentz force.

In our research, we have developed a simulation algorithm of carrier transport subject to Lorentz force in semiconductor films [3]. The Lorentz current is discretized with the drift and diffusion currents, and the simulation algorithm is implemented in finite difference methods. Hall effect around grain boundaries in poly-Si films is evaluated as a simulation example, and it is found that high Hall voltages are generated at the grain boundaries. Particularly in this presentation, we compare the Hall effect around the grain boundaries with different values of trap density.

DEVICE STRUCTURE

The device structure for the device simulation of the Hall effect around the grain boundaries in the poly-Si films is shown in Fig. 1. Here, the dopant species is n-type, the dopant density is $1 \times 10^{18} \text{ cm}^{-3}$, the carrier mobility is $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, a grain boundary exists at the center of the poly-Si film, the trap density at the grain boundary is 0.5×10^{13} or $1 \times 10^{13} \text{ cm}^{-2}$, the film width is 100 nm, the film length is 400 nm, the applied voltage is 1 mV, and the magnetic field is 0.1 T.

SIMULATION RESULTS

The spatial distributions of the electric potentials are shown in Fig. 2. It is found that high potential barriers are generated at the grain boundaries and spread to a few tens nm. Although this phenomenon has been reported in the previous article, it is confirmed that the simulation algorithm of carrier transport subject to Lorentz force does not spoil the conventional algorithm for the Poisson equation and drift and diffusion currents. Moreover, it is also found that as the trap density increases, the potential barrier becomes higher.

The spatial distributions of the Hall voltages are shown in Fig. 3. Here, the Hall voltages are defined as the difference of the electric potentials with and without the magnetic field. It is found that higher Hall voltages are generated at the grain boundaries than those in the grains. This is because the hall voltages are proportional to the carrier velocity, i.e., $V_H = vBW$. The carrier densities are lower owing to the potential barriers at the grain boundaries, and the carrier velocities are higher to maintain the conservation law of the electric current, i.e., Kirchhoff Law. Although the carrier mobility is the same, the electric fields at the grain boundaries are higher than those in the grains. As a result, the Hall voltages are higher at the grain boundaries. Moreover, it is also found that as the trap density increases, the potential barrier becomes higher, the carrier velocity becomes slower, and the Hall voltage becomes smaller. This phenomenon should be noted when the Hall effect is utilized to evaluate material properties in poly-Si films. The carrier mobility may be overestimated, and the carrier density may be underestimated.

REFERENCES

- [1] M. Kimura, et al., *Electrochem. Solid-State Lett.* **13**, J96 (2010).
- [2] Y. Yamaguchi, M. Kimura, et al., *IEEE Electron Device Lett.*, **31**, 1260 (2010).
- [3] M. Kimura, et al., *Solid State Electronics*, **63**, 137 (2011).

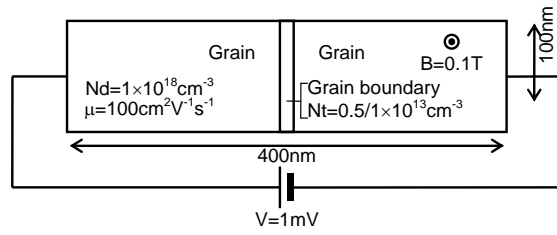
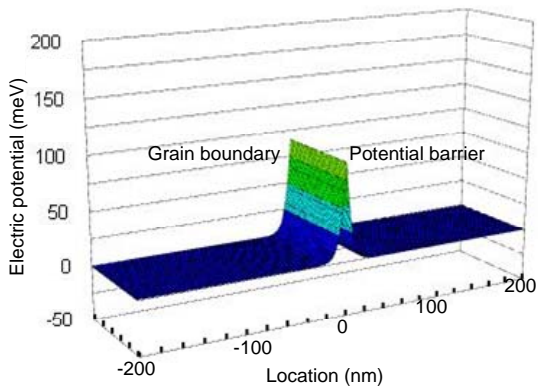
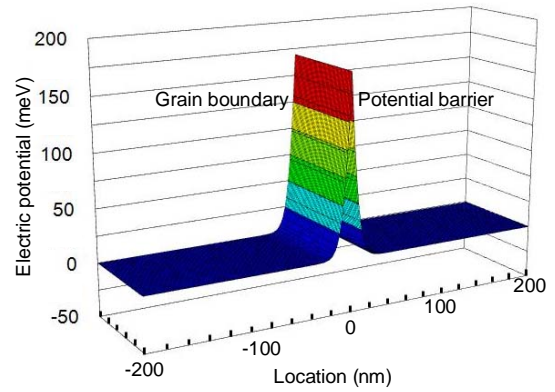


Fig. 1. Device Structure for the Device Simulation of the Hall Effect around the Grain Boundaries in the Poly-Si Films

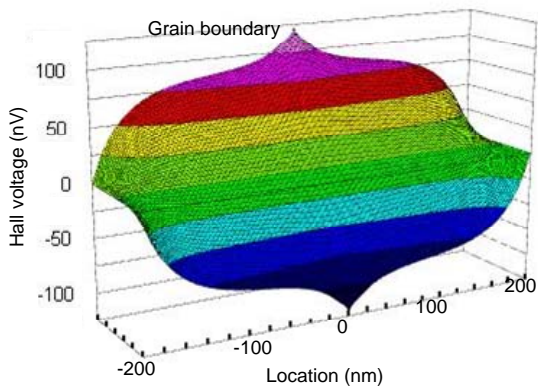


(a) Trap density = $0.5 \times 10^{13} \text{ cm}^{-2}$

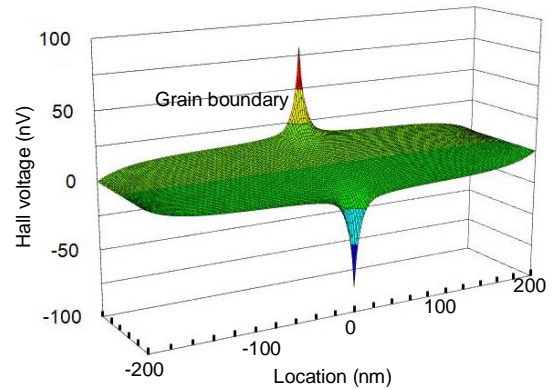


(b) Trap density = $1 \times 10^{13} \text{ cm}^{-2}$

Fig. 2. Simulation Results of the Spatial Distributions of the Electric Potentials around the Grain Boundaries



(a) Trap density = $0.5 \times 10^{13} \text{ cm}^{-2}$



(b) Trap density = $1 \times 10^{13} \text{ cm}^{-2}$

Fig. 3. Simulation Results of the Spatial Distributions of the Hall Voltages around the Grain Boundaries