A Compact Model for Wire-Type Tunnel FETs Considering Tunneling Path Lengths

Koichi Fukuda, Takahiro Mori, Wataru Mizubayashi, Yukinori Morita,
Akihito Tanabe, Meishoku Masahara, Tetsuji Yasuda, Shinji Migita, and Hiroyuki Ota
Collaborative Research Team Green Nanoelectronics Center (GNC),
National Institute of Advanced Industrial Science and Technology (AIST)
16-1 Onogawa, Tsukuba, Ibaraki 305-8569, JAPAN

Tunnel FET (TFET) is one of the key devices for low-power applications beyond CMOS [1]. However studies of TFET circuits are still in early stage because of the lack of a TFET compact model. Authors have reported a compact model of TFETs based on the nonlocal band to band tunneling (BTBT) model [2]. In this paper, the model is expanded to fin (double gate) and wire-type (cylinder) TFETs.

In the previous model in ref. [2], tunneling path is divided into two parts, vertical path at source gate overlap region, and horizontal path along gate insulator interface as shown in fig.1. The model agrees well with measured IV-curves (fig.2) of SOI-type planar TFETs developed by our group [3].

Since the key difference of the present model is the lateral potential profile along the gate insulator interface, the vertical profile considered in the previous work is not discussed in this paper. In our model, the potential profile is expressed by position dependent capacitances of each point along the gate insulator interface given by

$$\psi(x) = \frac{V_{source} \cdot C_{source}(x) + V_{gate} \cdot C_{gate}(x)}{C_{source}(x) + C_{gate}(x)} \qquad (1)$$

where *x* denotes the distance from the source junction. The source and the gate capacitances of each point are obtained by numerical simulations and fitted to the following equations,

$$C_{gate}(x) \sim \frac{ax + b}{x + c} + F_{correction}(x) \qquad (2)$$

$$C_{source}(x) \sim \frac{d}{x^e + f} \cdot G_{correction}(x) \qquad (3)$$

Where *a~f…* are fitting parameters and *Fcorrection* and *Gcorrection* are correction functions to realize better accuracy. Simulated and fitted capacitances are compared in fig.3. Strong interaction is observed between the two capacitance components. This is the reason why eq. (2) and (3) require correction terms. Potential profiles obtained from the model are compared with simulations in fig.4. Wire-type TFET provides steeper potential profiles than fin-type does, and the steepness is increased by decreasing their feature sizes.

The tunnel distance $\lambda_{tunnel}(x)$ is obtained by

$$\psi\big(x + \lambda_{tunnel}(x)\big) = \psi(x) + E_g \qquad (4)$$

where *Eg* is the bandgap. This $\lambda_{tunnel}(x)$ is used to calculate BTBT rates using Kane's formula.

$$G_{BTBT}(x) = A \cdot E^p \cdot exp\left(-\frac{\lambda_0}{\lambda_{tunnel}(x)}\right) \qquad (5)$$

The drain current of TFET is obtained by,

$$I_d = \int G_{BTBT} dV \qquad (6)$$

I-V curves of fin, wire and SOI-type silicon TFETs predicted by the present model are shown in fig.5. Steepness of the curves are better in an order of Wire > Fin > SOI. Drain saturation currents *Idsat* at the same gate bias is plotted as a function of fin-thicknesses or wire-diameters in fig.6. It should be mentioned that wire-type TFETs provide larger currents even in large wire diameters such as 50nm. This comes from the fact that wire-insulator interfaces are surrounded by the gate.

Eq. (1)~(6) are ready for implementations to our compact model of TFET described by Verilog-A languages. Thus we have built a basis for a set of TFET compact models consistent for bulk, SOI, Fin and Wire types.

ACKNOWLEDGEMENT

This research is granted by JSPS through FIRST Program initiated by CSTP.

REFERENCES

[1] Adrian M. Ionescu, Heike Riel, Nature 479, pp.329–337, 2011.
[2] K.Fukuda et al., Extended Abstract of SSDM, p.799 ,2012.
[3] T.Mori et al., Extended Abstract of SSDM, p.74, 2012.

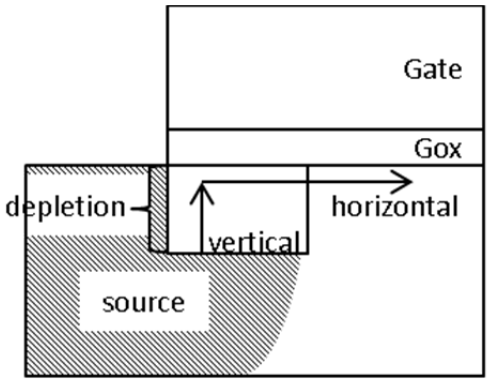

Fig. 1. Concept of the path length assumption in our model. The tunnel path is divided into two parts. This paper focuses on the horizontal tunnel path.

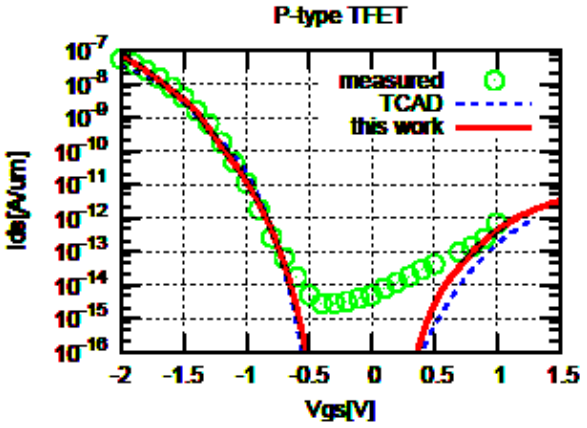

Fig. 2. Comparison of our model in ref. [3] with a measured IV curve of TFET fabricated by our group.

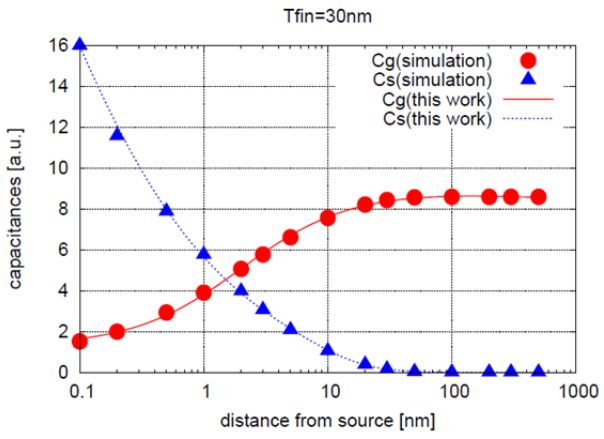

Fig. 3. Capacitances of the model and simulation results. Source and gate capacitances affect each other.

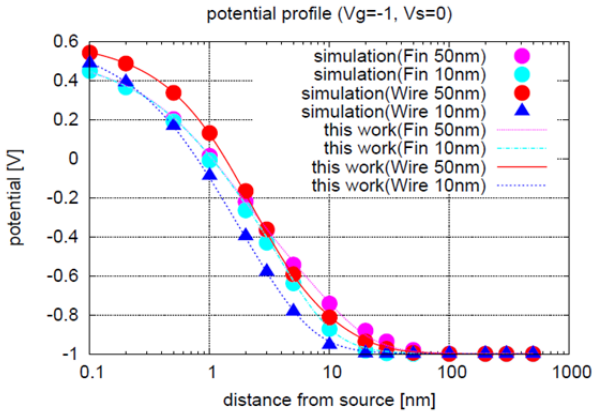

Fig. 4. Lateral potential profile compared with numerical simulation results. Potential profiles of wire-TFETs are steeper than those of fin-TFETs.

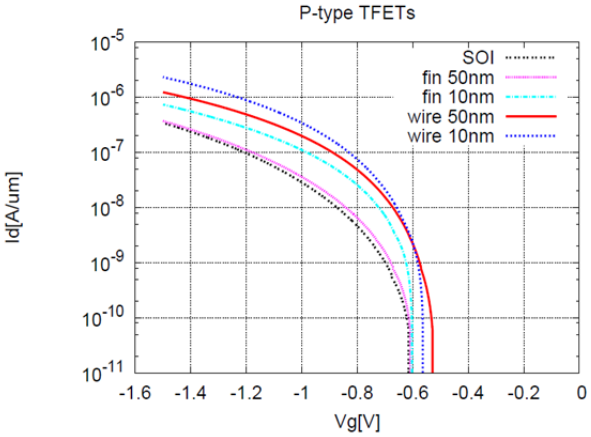

Fig. 5. Id-Vg characteristics predicted by the present model. Scaling merit is observed stronger in wire-TFETs.

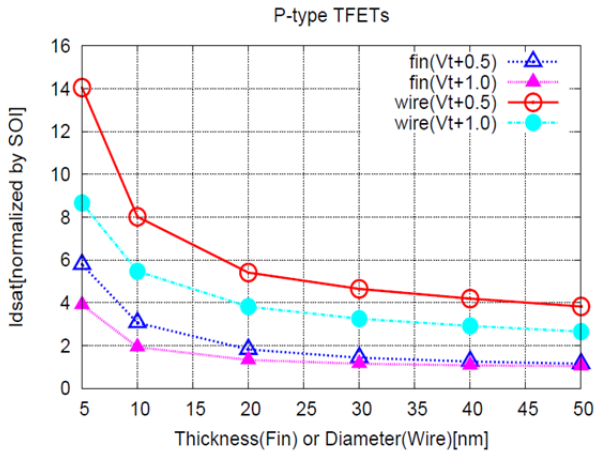

Fig. 6. Size scaling merits of saturation current at *Vg=Vt-0.5*, *Vt-1.0* (*Vt* @ Id=10^{-11}[A/um]) of fin and wire-type TFETs. Currents are normalized by those of SOI-TFETs.