

Reduction of Self-Heating Effect in CMOS Inverter of Vertical MOSFET by Common-Gate Layout

A. Wang^{1,2}, and T. Endoh^{1,2}

¹Graduate School of Engineering, Tohoku University, ²JST-CREST
Aramaki Aza-Aoba 6-6, Aoba-ku, Sendai, Japan, 980-8579, E-mail: endoh@riec.tohoku.ac.jp

INTRODUCTION

Very Large Scale Integration (VLSI) shows higher performance by improving the density year by year. However, higher density of VLSI induces a large current density, leading the increase of temperature in a circuit, which will degrade the performance of the circuit [1]. Therefore, it is important to restrain the self-heating effect in a circuit. One of efficient solvents to this problem is designing a high efficient heat dissipation layout of the circuit considering self-heating effect. In this paper, 22nm technology node CMOS Inverter composed of Vertical MOSFET [2,3] is investigated considering both electrical and thermal properties. It is clarified by 3D device simulation results that Vertical NMOS drain side is the hot spot and gate is one of the dominant heat radiation routes from the hot spot. It is also shown that common-gate layout have a thermal advantage than separate-gate layout by dissipating much heat from the hot spot.

SIMULATION METHOD

Figure 1 (a) and (b) show the layout of common-gate CMOS Inverter and separate-gate CMOS Inverter of Vertical MOSFET in the same footprint ($17F \times 7F$). Table I shows the parameters used in the 3D device simulation. We assume the most severe thermal situation for the circuit, the case that all adjacent circuits are active. We attached thermal resistances equivalent to 12 layers of interconnect above the top of the simulation area (M1 metal) and 50 μ m Si substrate below the bottom of the simulation area.

RESULTS AND DISCUSSION

Figure 2 shows the power of two layout types are the same under dc operation when input voltage

(V_{in}) from 0.4V to 0.55V, which shows the most high power due to the through current (I_T). When V_{in} is 0.46V, NMOS drain side shows the peak temperature (423K) as shown in Fig. 3. This is due to the difference of current density between NMOS and PMOS. It is important to release the heat from NMOS drain side, the hot spot in entire simulation area to maintain the performance of the circuit. Figure 4 shows the heat flux distribution when V_{in} is 0.46V. As from this figure, the heat of NMOS drain side dissipates via high thermal conductivity material tungsten (W) and silicon (Si) area. Particularly, in our simulation situation, dominant heat radiation routes are the paths toward drain contact, source contact and gate. Conducting much heat via gate, common-gate layout shows around 3% reduction of temperature raise than the separate-gate layout as shown in Fig. 5.

CONCLUSION

The self-heating effect in CMOS Inverter composed of Vertical MOSFET is analysed for the first time. It is shown that NMOS drain side is the hot spot in the circuit. Thus, it is important to dissipate heat from the NMOS drain side. One of the dominant heat radiation routes from NMOS drain side is gate. Thus, the common-gate layout for CMOS Inverter composed of Vertical MOSFET shows 3% reduction of temperature raise by conducting much heat from NMOS drain side to PMOS via gate, which is important to maintain high reliability of the circuit.

ACKNOWLEDGEMENT

This work has been supported in part by a grant from "Research of Innovative Material and Process for Creation of Next-generation Electronics Devices" of CREST under the Japan Science and Technology Agency (JST).

REFERENCES

- [1] Semenov, O. et al., IEEE Transactions on , vol.6, no.1, pp. 17- 27, March 2006
- [2] T. Endoh, T. Nakamura, and F. Masuoka, IEICE Trans. on Electronics, Vol.E80-C, No.7, pp.911-917, July 1997
- [3] T. Endoh, K. Tanaka, Y. Norifusa, IEICE Trans. Electron, Special Issue on Fundamentals and Applications of Advanced Semiconductor Devices,2008

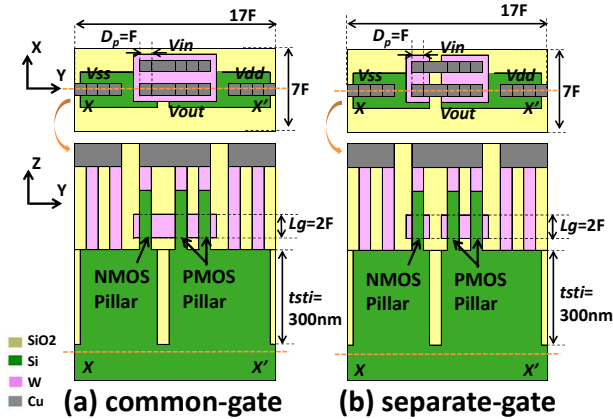


Fig. 1. (a) Layout of Common-Gate CMOS Inverter and (b) Separate-Gate CMOS Inverter of Vertical MOSFET.

Table I. Parameters for this simulation.

Parameters	
Feature Size (F)	22nm
Pillar Diameter (D_p)	F (=22nm)
Gate Length (L_g)	$2F$ (=44nm)
Gate Oxide Thickness (t_{ox})	1.2nm
STI thickness (t_{sti})	300nm
Ambient Temperature (T_{amb})	400K
Power Supply (V_{dd})	0.9V

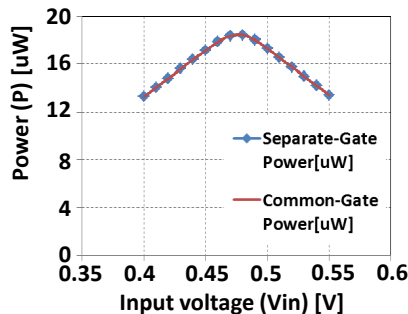


Fig. 2. Power for Vertical CMOS Inverter under dc operation due to the through current, where $P = V_{dd} \times I_T$. Here, V_{dd} is supply voltage and I_T is through current.

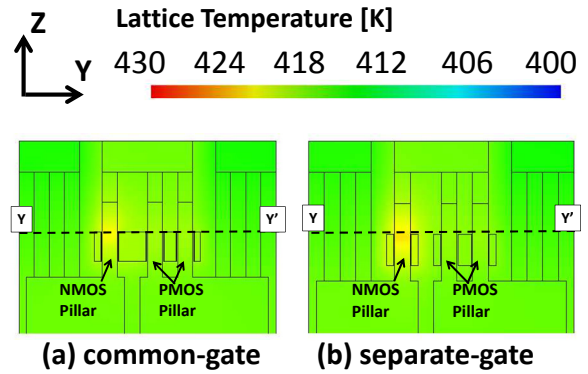


Fig. 3. Lattice temperature distribution under dc operation for (a) common-gate layout and (b) separate-gate layout when the bias recorded the highest peak temperature ($V_{in} = 0.46V$).

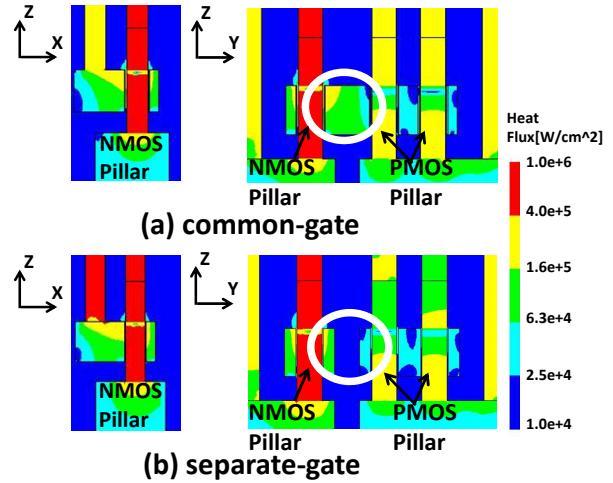


Fig. 4. Heat flux distribution for (a) common-gate layout and (b) separate-gate layout when the bias recorded the highest peak temperature ($V_{in} = 0.46V$).

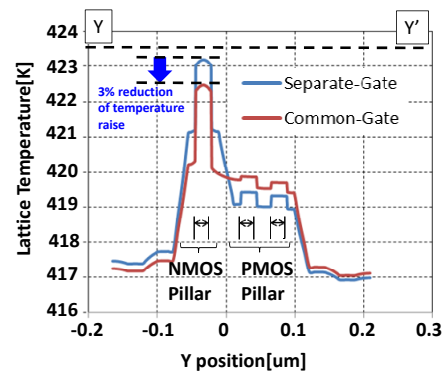


Fig. 5. Lattice temperature distribution for the cross-sectional view along the line Y-Y' in Fig. 3, under dc operation when the bias recorded the highest peak temperature ($V_{in} = 0.46V$), temperature raise: the rise of temperature from 400K.