Quantum Simulation of III-V Double Gate Schottky Barrier MOSFETs

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INTRODUCTION

Schottky barrier metal-oxide-semiconductor field-effect transistors (SB-MOSFETs) are one of the promising candidates for the future nano-scaled devices [1]. They have advantages of suppressing short channel effects due to low resistivity of ultra-shallow junction at source/drain. However, a major drawback of SB-MOSFETs is that on-state current (I_{on}) is considerably lower compared to conventional MOSFETs because SB-MOSFETs are operated by tunneling current (I_{tunn}) through SB [2]. In an attempt to enhance I_{on}, we proposed to adopt III-V materials as channel material such as InAs and GaAs which have small effective masses (m_{eff}), $0.023m_0$ and $0.063m_0$ in bulk, respectively. But the following issues are present with III-V SB-MOSFETs: III-V materials with narrow bandgap (E_g) such as InAs may suffer from high off-state current (I_{off}) [3], while those with wide E_g such as GaAs have a high SB height (SBH). In this work, we assess the performance limits of ultra-thin-body (UTB) III-V SB-MOSFETs compared with Si SB-MOSFETs.

SIMULATION APPROACH

The structure of double-gate UTB SB-MOSFETs is shown in Fig. 1. To describe the electron transport, the effective mass Hamiltonians were used with the effective masses adjusted by the $sp^3d^5s^*$ tight-binding method. The adjustment is crucial to properly take into account the quantization effect (QE) in UTB structure.

In this work, the electron transport was treated fully quantum mechanically because precise calculation of I_{tunn} is important in SB-MOSFETs. The electron density and potential were calculated by solving the non-equilibrium Green's function equation and Poisson's equation self-consistently [2]. Note that, although we focused on the electron transport in this work, we also calculated hole current to treat the ambipolar behavior of SB-MOSFETs and determine I_{off}. The six-band $k{\cdot}p$ Hamiltonian was used for hole transport calculation.

RESULTS AND DISCUSSION

The drain current (I_d) versus gate voltage (V_g) characteristics of InAs, GaAs, and Si SB-MOSFETs with T = 5nm are shown in Fig. 2. The gate length (L_g) is scaled as $L_g = 4T$, where T is a thickness of UTB, and equivalent oxide thickness (EOT) and SBH are 1nm and 0eV, respectively. The drain voltage (V_d) of 0.5V is applied.

Fig. 3 (a) shows I_d at the saturation region ($I_{d,sat}$) as W is decreased. $I_{d,sat}$ is defined as I_d when the minimum value of channel potential coincides with the value of potential at the top of drain-SB. Due to the low transconductance (See Fig. 2.), $I_{d,sat}$ of III-V SB-MOSFETs is less than that of Si SB-MOSFETs, which is contrary to expectation. Note that $I_{d,sat}$ of III-V SB-MOSFETs increases with W while that of Si SB-MOSFETs decreases. The latter is due to the usual behavior that the gate controllability becomes worse as W is increased. The reason for the former is the strong QE occurs due to small m_{eff}, which makes the effective SBH to increase and the number of subband to decrease. See Figs. 3 (c) and (d). The above QE can also explain that $I_{d,sat}$ of InAs SB-MOSFETs increases more steeply than that of GaAs SB-MOSFETs as shown in Fig. 3 (b).

The I_{on} and I_{off} versus W are shown in Fig. 4 (a) for the three channel materials. I_{on} was calculated with V_d after adjusting the gate work function such that $I_{off} = 0.1\mu A/\mu m$. If I_{off} does not satisfy with the criteria, it was measured by the lowest I_d in the ambipolar current graph. At T = 10nm, both InAs and GaAs SB-MOSFETs show higher I_{on} in comparison to Si SB-MOSFETs. However, InAs SB-MOSFETs show drastic decrease of I_{on} upon reduction of T. On the other hand, as shown in Fig.

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4 (b), I_{on}/I_{off} of InAs SB-MOSFETs becomes remarkably worse as T is increased, due to the fact that I_{off} increases sharply.

In InAs SB-MOSFETs, high I_{off} seriously limits the performance. We, therefore, propose to use gate underlap as a solution to improve the I_{off} behavior. Fig. 5 (a) shows the dependence of the I_{on}, I_{off}, and I_{on}/I_{off} on the gate position with the channel length (L_{ch}) of 25nm. Regardless of the gate position, SB-MOSFETs with gate underlap make both I_{on} and I_{off} to decrease. However, when the gate is placed near the source (underlap length: L_{u1} = 0nm and L_{u2} = 5nm, respectively; see Fig. 1 for the definition of L_{u1} and L_{u2}), I_{on} is comparable to the case with no underlap while I_{off} becomes lower. The dependence of I_{on}, I_{off}, and I_{on}/I_{off} of InAs SB-MOSFETs on L_{u2} is shown in Figs. 5 (b) and (c). We conclude that, as L_{ch} is increased (with L_{u1} and L_g fixed), I_{on}/I_{off} is improved exponentially.

Fig. 5 (d) shows the I_{on} versus SBH for GaAs and Si SB-MOSFETs with T = 5nm. Recall that SBH is set to 0V for all the materials considered in this work. Since the typical SBH for GaAs is 0.6eV, methods to lower SBH should be devised.

CONCLUSION

For the purpose of enhancing the performance of SB-MOSFETs, III-V materials having small m_{eff} such as InAs and GaAs are investigated. We have found that the enhancement in III-V SB-MOSFETs can be limited by I_{off} for narrow E_g materials. As a solution to overcome it, gate underlap has been suggested and its effect on the improvement on I_{off} has been investigated.

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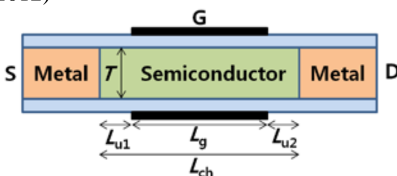

Fig. 1. The schematic diagram of UTB SB-MOSFETs.

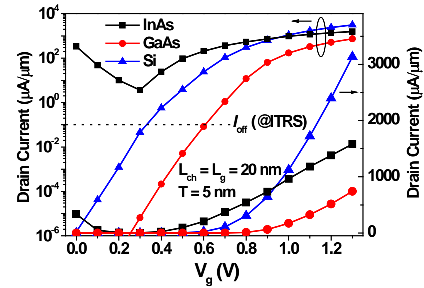

Fig. 2. I_d-V_g characteristics of InAs, GaAs, and Si SB-MOSFETs with T = 5 nm and L_g = 20 nm, displayed in the log scales (left axis) and linear scales (right axis).

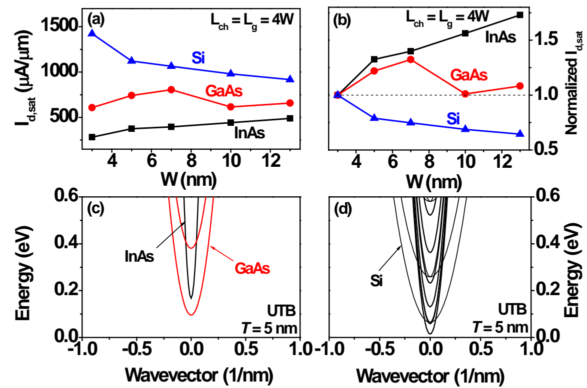

Fig. 3. (a) $I_{d,sat}$ and (b) normalized $I_{d,sat}$ of InAs, GaAs, and Si SB-MOSFETs are shown as W varies from 13nm down to 3nm. The figure shows the conduction subband structure of 5 nm thickness with (c) InAs, GaAs, and (d) Si channel. Energy is measured with reference to the bulk conduction band minima.

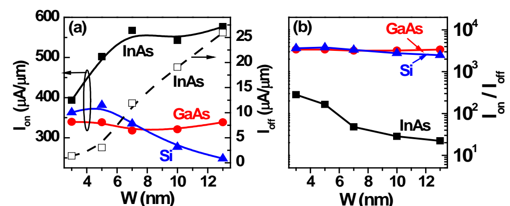

Fig. 4. The dependence of (a) I_{on}, I_{off} (InAs only), and (b) I_{on}/I_{off} on W is shown.

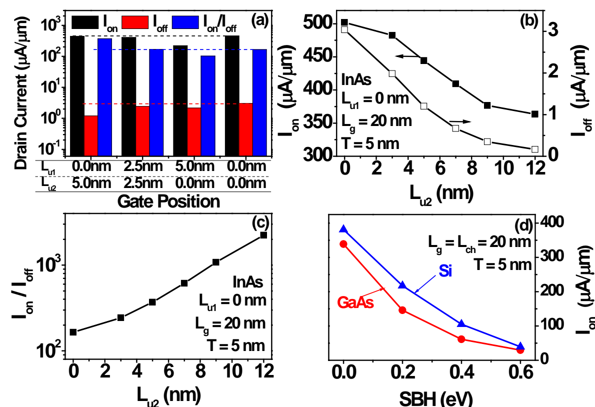

Fig. 5. (a) The graph shows the dependence of I_{on}, I_{off}, and I_{on}/I_{off} of InAs SB-MSFETs with gate underlap (L_{ch} = 25nm) and no underlap (L_{ch} = L_g = 20nm) on the gate position. (b) I_{on}, I_{off}, and (c) I_{on}/I_{off} versus L_{u2} of InAs SB-MOSFETs with asymmetric gate underlap are shown. (d) I_{on} of GaAs and Si SB-MOSFETs is shown as SBH varies from 0.0eV to 0.6eV.