Thickness dependent performance of (111) GaAs UTB nMOSFETs

K. Alam, S. Takagi, and M. Takenaka
Department of Electrical Engineering and Information Systems
The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan
e-mail: kalam@mosfet.t.u-tokyo.ac.jp, takagi@ee.t.u-tokyo.ac.jp

Electron transport in III-V semiconductors such as GaAs, InAs, GaSb, and InGaAs has drawn significant attentions due to high electron injection velocity (good side) and low density-of-states (DOS) (bad side) [1]–[3]. A solution to DOS bottleneck has been proposed by quantizing an ultra-thin-body (UTB) channel along the crystallographic <111> direction [3]–[6]. Using an atomistic tight binding (TB) top-of-the-barrier (ToB) model, Mehrotra *et al.* [4] have shown that a 2 nm thick (111) GaAs channel outperforms (100) Si and GaAs channels for an effective oxide thickness (EOT) larger than 0.3 nm. Studies on different orientations by Luisier [3] and Kim *et al.* [6] show that (111) GaAs and GaSb UTB channels outperform Si and Ge. In this work, the thickness dependent performance of a (111) GaAs UTB nMOSFET is studied using a ToB model that self-consistently solves $sp^3s^*d^5$ orbital basis Hamiltonian for electron density and two dimensional Poisson's equation for electrostatics. The Hamiltonian includes spin-orbit interaction and uses energy parameters of [7]. The device performance improves up to the UTB thickness of $\approx$ 3 nm and then it degrades.

A few conduction bands of (111) GaAs UTBs are shown in Fig. 1 for two different values of UTB thickness, T_{utb}. At thicker T_{utb}, the quantized L valley projects at a higher energy, Fig. 1(a), and the transport is primarily governed by the single Γ valley subband. With thinner T_{utb}, Fig. 1(b), the two valley subbands align in energy leading to many modes for transport.

The current-voltage characteristics for three T_{utb} are shown in Fig. 2. We use an EOT of 0.5 nm and a V_{DS} of 0.6 V. For performance comparison at the same gate bias, a potential barrier height of 0.5 eV is set at V_{GS} = 0 V for all the devices. At lower gate biases, the transport in 6.77 nm UTB is through the single mode from Γ valley (see Fig. 1 (a)). For 2.86 nm UTB, many modes from projected L valley get populated and the current is much higher. With increased bias, high energy modes of 6.77 nm UTB also get populated and the current is improved. For the 6.77 nm and 4.81 nm UTBs, the current at zero gate bias is almost same due to single mode transport. At intermediate biases, the current in 4.81 nm UTB is higher due to lower Γ-L energy separation. Finally, at very high gate biases, the current in both the UTBs is almost same due to significant population of the high energy modes.

In Figs. 3 and 4, we plot the current, electron sheet density, quantum capacitance, and the switching delay versus T_{utb} at a gate bias of 1.0 V. We choose this gate bias to make sure that all the devices operate in saturation. In the plots, the device performance improves with thinner channel until $T_{utb} \approx 3$ nm. Beyond this thickness, the performance slightly degrades. This degradation is due to the double role of quantization. When $T_{utb} > 3$ nm, the Γ-L energy separation is reduced with thinner UTB. This increases the number of available modes within the energy range of interest and the device performance is improved. When $T_{utb} < 3$ nm, the lowest energy mode comes from L valley and the energy separation between the low energy modes is increased with thinner UTB. This reduces DOS, Fig. 5, and the device performance is degraded.

In summary, the double role of quantization is important in device design of (111) GaAs UTB nMOSFETs, especially for very thin channel.

ACKNOWLEDGMENT

This work was supported by Japan Society for Promotion of Sciences (JSPS) fellowship.

REFERENCES

[1] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, "Advanced high-K gate dielectric for high-performance short-channel $In_{0.7}Ga_{0.3}As$ quantum well field effect transistors on silicon substrate for low power logic applications," in *Int. Electron Dev. Meet.* Baltimore, Maryland: IEEE, 2009, pp. 319–322.

978-3-901578-26-7

[2] M. Fischetti, L. Wangt, B. Yut, C. Sachs, P. M. Asbeck, Y. Taurt, and M. Rodwell, "Simulation of electron transport in high-mobility MOSFETs: Density of states bottleneck and source starvation," in *International Electron Devices Meeting*, 2007, pp. 109–112.

[3] M. Luisier, "Performance comparison of GaSb, strained-Si, and InGaAs double-gate ultrathin-body n-FETs," *Electron Dev. Lett.*, vol. 32, no. 12, pp. 1686–1688, 2011.

[4] S. Mehrotra, M. Povolotskyi, J. Lawy, T. Kubis, G. Klimeck, and M. Rodwell, "Design of high-current L-valley GaAs/AlAs$_{0.56}$Sb$_{0.44}$/InP(111) ultra-thin-body nMOSFETs," in *International Conference on Indium Phosphide and Related Materials*, University of California, Santa Barbara, 2012.

[5] M. Rodwell, W. Frensley, S. Steiger, E. Chagarov, S. Lee, H. Ryu, Y. Tan, G. Hegde, L. Wang, J. Law, T. Boykin, G. Klimek, P. Asbeck, A. Kummel, and J. Schulman, "III-V FET channel designs for high current densities and thin inversion layers," in *Device Research Conference (DRC)*, 2010, pp. 149–152.

[6] R. Kim, T. Rakshit, R. Kotlyar, S. Hasan, and C. E. Weber, "Effects of surface orientation on the performance of idealized III-V thin-body ballistic n-MOSFETs," *Electron Dev. Lett.*, vol. 32, no. 6, pp. 746–748, 2011.

[7] T. B. Boykin, G. Klimeck, R. C. Bowen, and F. Oyafuso, "Diagonal parameter shifts due to nearest-neighbor displacements in empirical tight-binding theory," *Phys. Rev. B*, vol. 66, no. 12, p. 125207, 2002.

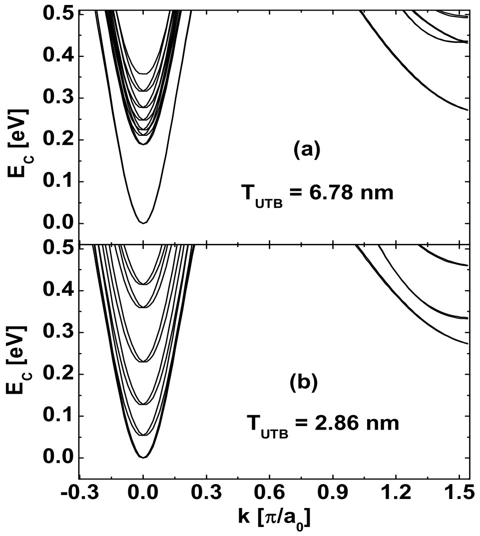

Fig. 1: A few conduction bands of the (111) GaAs UTB for two different values of UTB thickness. The conduction band bottom has been shifted to 0 for comparison. In the plots, positive k: $\Gamma - X$ and negative k: $\Gamma - L$.

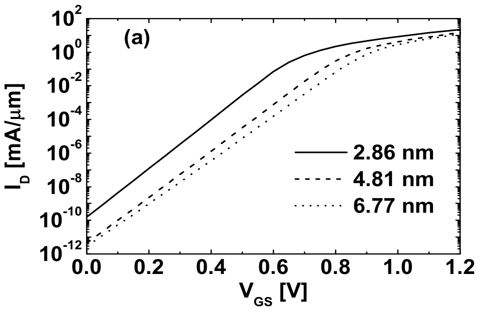

Fig. 2: Current-voltage characteristics for three different values of UTB thickness.

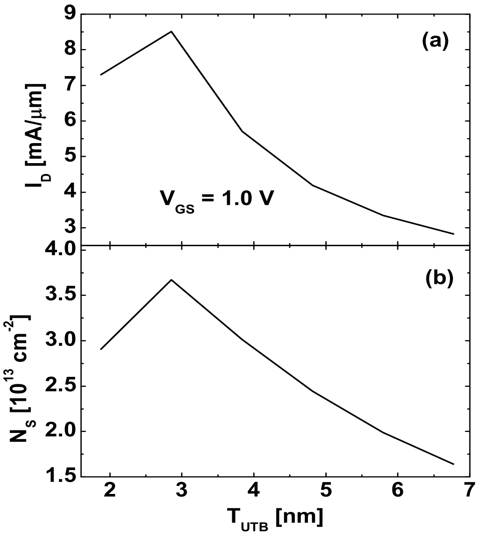

Fig. 3: Current and electron sheet density versus UTB thickness at a gate bias of 1.0 V.

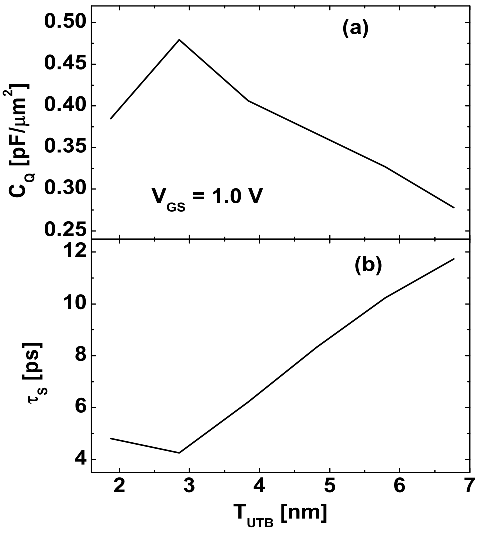

Fig. 4: Quantum capacitance and switching delay versus UTB thickness at a gate bias of 1.0 V.

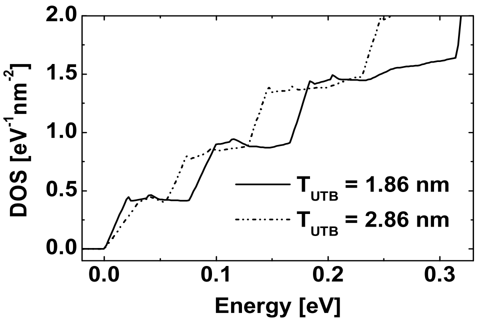

Fig. 5: Zero bias density of states at two different values of UTB thickness. Energy 0 is the conduction band bottom.