Molecular-Metal-Oxide-nanoelectronicS (M-MOS): Achieving the Molecular Limit

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INTRODUCTION

In recent years interest in electronic, magnetic and optical structures and devices based on inorganic, organic, hybrid and nano-materials has increased significantly. An example of this is the EPSRC funded M-MOS Programme Grant, which provides an exciting opportunity for research in the field of molecular electronics based on hybrid nano-materials. Among the aims of this project is to study extensively, using 3D simulations, the interplay between variability, scalability and reliability of a non-volatile flash-memory cell, in which the charge-storing components constitute of a layer of polyoxometalates molecular clusters (POMs) – Fig.1. POMs are metal-oxide inorganic molecules formed by early transition metal ions and oxo ligands [1] – Fig.2. Importantly, they can undergo multiple times reversible reduction/oxidation, which makes them attractive candidates for multi-bit storage in flash memory cells. The use of redox-active molecules to form the floating gate (FG) could offer several very important advantages over the conventional polysilicon FG [2].

DISCUSSION

In order to evaluate the idea of POMs, based non-volatile molecular memories, we developed a simulation flow that links the density functional theory (DFT) result to three-dimensional (3D) numerical flash cell simulations – Fig.3. The custom-built *Simulation Domain Bridge*, which establishes a connection between the two distinct modelling schemes (DFT for the molecular part and mesoscopic device modelling for the flash cell), was a vital step in this flow.

For the purpose of this paper we have designed an 18 nm x 18 nm square gate n-channel flash memory cell. The gate dielectric is assumed to be SiO_2 with thickness of 20 nm. The POMs layer is 4.5 nm above the Si substrate, where 3 nm are SiO_2 and 1.5 nm is balancing cation from the insulation barrier (see green chains in Fig.2). The molecular layer has a 4x4 rectangular planar arrangement of the POMs.

Using a floating gate built from 4x4 POMs with molecular formula $[W_{18}O_{54}(SO_3)_2]^{4-}$, arranged in a planar distribution, we calculated the drain current of the cell – Fig.4. The main assumption is that all of the POMs within the layer are simultaneously reduced by one (blue line) or two (red line) electrons. Adding (reducing) additional negative charges into the FG leads to lowering of the source-drain current and to a threshold voltage shift. Fig.5 reveals the increase of the threshold voltage, ΔV_{TH}, as a function of the sheet-charge density. ΔV_{TH} agrees well with the idealised analytical model. Moreover, reducing each POM by two electrons produces the same impact on V_{TH} as doubling the sheet density in the analytical dependence. A directly link can be established between the results presented in Fig.5 and the potential barrier profile along the channel shown in Fig.6. The height of the barrier in the channel determines the shift in ΔV_{TH}.

REFERENCES

[1] D.-L. Long, Y.-F. Song, E. F. Wilson, P. Kögerler, S.-X. Guo, A. M. Bond, J. S. J. Hargreaves, L. Cronin, *Angew. Chem. Int. Ed.* **47**, 4384-4387 (2008).
[2] J. Lee, S. H. Hur, J.-D. Choi, *IEEE Electron Device Letters* **23/5**, 264-266 (2002).

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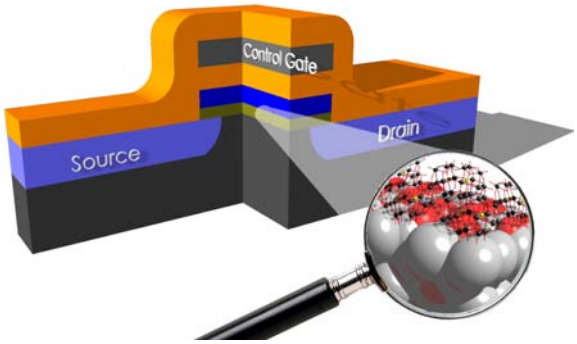

Fig. 1. Schematic representation of a single-transistor non-volatile memory cell, showing an array of polyoxometalate clusters (POMs) as part of the floating gate.

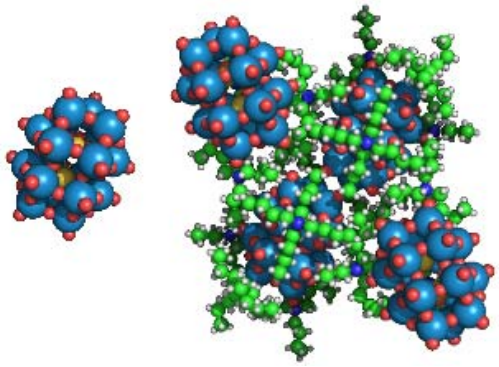

Fig. 2. Schematic representation of POMs cluster anions, $[W_{18}O_{54}(SO_3)_2\ ]^{4-}$, with their cations (green chains). Colour scheme: O, red; W, blue; Se, yellow.

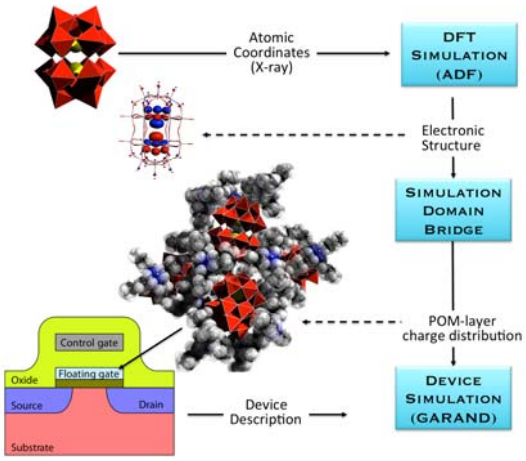

Fig. 3. Simplified block diagram of the simulation methodology, linking DFT and flash-cell modelling. The simulation domain bridge is developed in-house. The commercial simulators ADF and Garand are used for the DFT and three-dimensional device simulations respectively.

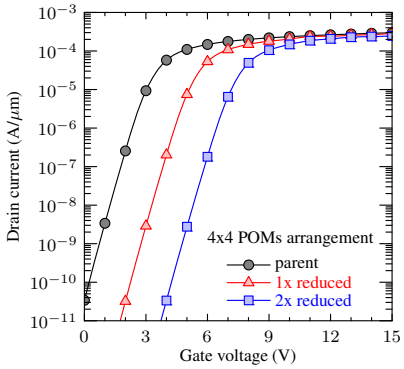

Fig. 4. Clear lowering of the source-drain current corresponding to the reduction of each POM simultaneously by 1(blue) and 2(red) electrons. The centres of all POMs are 4.5nm above the substrate.

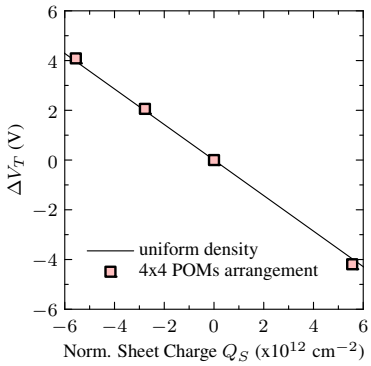

Fig. 5. Comparison of the threshold voltage shift ΔV_{TH} due to an idealised sheet charge in the oxide (line), and due to a POM-FG (symbols), versus sheet charge density (normalised by the electron charge).

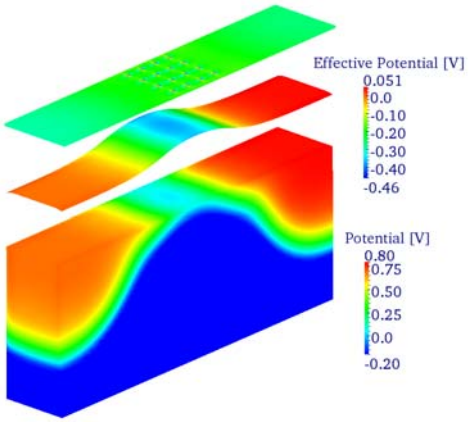

Fig. 6. Potential barrier profile along the channel of the flash-cell (2D elevated plot) and distribution of the effective potential of the simulated device (3D). Fingerprints of the twelve POMs placed in the floating gate are visible on the top (green) panel above the potential barrier profile along the channel.