Improvement of Self-Heating Effect Employing Vertical-Channel Field-Effect-Diode 1T-DRAM

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INTRODUCTION

Capacitorless 1T-DRAM has been developed to overcome the scaling limitations of conventional 1 transistor 1 capacitor DRAM cells [1]. Previously, we proposed the Field Effect Diode (FED) type vertical 1T-DRAM with negative hold Bit Line (BL) voltage scheme for excellent hold characteristics and low voltage operation [2]. In this paper, the excellent thermal characteristics of our proposed 1T-DRAM compared to the conventional vertical channel 1T-DRAM using Single Transistor Latch (STL) [3] are analyzed in detailed through Sentaurus 3-D device simulator [4] including the Self-Heating Effect (SHE).

MEMORY CELL STRUCTURE AND OPERATION VOLTAGES

Figure 1 (a) and (b) show the schematics of the conventional STL type vertical 1T-DRAM and the FED type vertical 1T-DRAM. The STL type is based on the vertical double gate MOSFET. On the other hand, the FED type is based on the vertical cylindrically p-i-n diode with surrounding gate. Both the STL type and the FED type, an ideal cell size of $4F^2$ can be achieved due to vertical structure. Simulated memory cell design parameters and memory cell operation voltages are shown in Table I and II. Because the highest BL voltage (V_{BL}) is applied in the whole memory operation, the transient thermal characteristics of write “1” operation are focused in this study.

EVALUATION OF SELF-HEATING EFFECT IN THE STL TYPE AND THE FED TYPE 1T-DRAM

Write “1” operation of the STL type and the FED type 1T-DRAM are shown in Fig. 2 and Fig. 3. In the STL type, maximum lattice temperature in the memory cell increased 143K and reaches the value of 443K at 45nsec as BL current (I_{BL}) is increased. Moreover, as maximum lattice temperature is increased, I_{BL} is also increased. This feedback effect is due to the intrinsic bipolar effect. On the other hand, the FED type shows the excellent thermal characteristics. After V_{BL} is applied to -1.1V, $|I_{BL}|$ increases sharply while the STL type increases gradually. In the FED type, peak value of the maximum lattice temperature is only 301.2K at 46nsec with 1.2K rise of temperature. Figure 4 (a) and (b) show the hole distribution along the channel direction of the STL type and the FED type. Hole can be stored under the G_1 within 60nsec access time. Lattice temperature distributions in the memory cell after write “1” operation (time=60nsec) are shown in Fig. 5. In the STL type, maximum lattice temperature is reached 352K while the FED type is reached 300.3K. From all, it is shown that the FED type shows excellent thermal characteristics and can nearly avoid SHE.

CONCLUSION

Excellent thermal characteristics of the FED type 1T-DRAM are presented for the first time by comparing to the conventional STL type 1T-DRAM. Vertical channel type FED 1T-DRAM has the potential to extend scaling limitations.

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REFERENCES

[1] T. Ohsawa, et al., *IEEE J. Solid-State Cir.*, pp. 1510-1522, 2002.
[2] T. Imamoto, et al., Ext. Abs. Int. Conf. SSDM, 2012, pp.588-589
[3] W. Kwon, et al., Jpn. J. Appl. Phys. 49 2010.
[4] http://www.synopsys.com/

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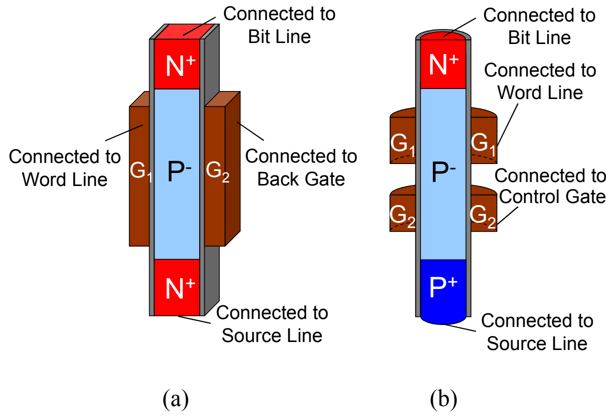

Fig. 1. The schematics of the vertical channel capacitorless 1T-DRAM cell. (a) Single Transistor Latch (STL) type and (b) Field Effect Diode (FED) type.

Table I. Memory cell design parameters.

Parameter	STL type	FED type
Silicon thickness (T_{Si})	20nm	
Silicon pillar diameter (D)		20nm
Gate length (L_G)	50nm	60nm
Control Gate length (L_{CG})		50nm
Oxide thickness (T_{OX})	5nm	

Table II. Memory cell operation voltages.

	STL type		FED type	
	WRITE"1"	HOLD	WRITE"1"	HOLD
V_{BL}	2.0V	0.0V	-1.1V	-0.6V
V_{WL}	-1.0V	-2.0V	0.0V	-2.0V
V_{CG}			0.3V	
V_{BG}	1.0V			
V_{SL}	0.0V			
V_{Sub}	0.0V			

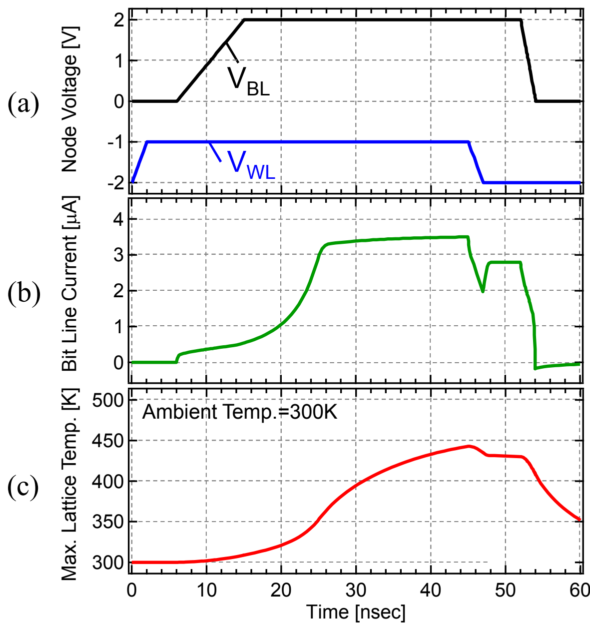

Fig. 2. Write "1" operation of the STL type 1T-DRAM cell. (a) Node voltage (b) Bit line current and (c) Maximum lattice temepratur.

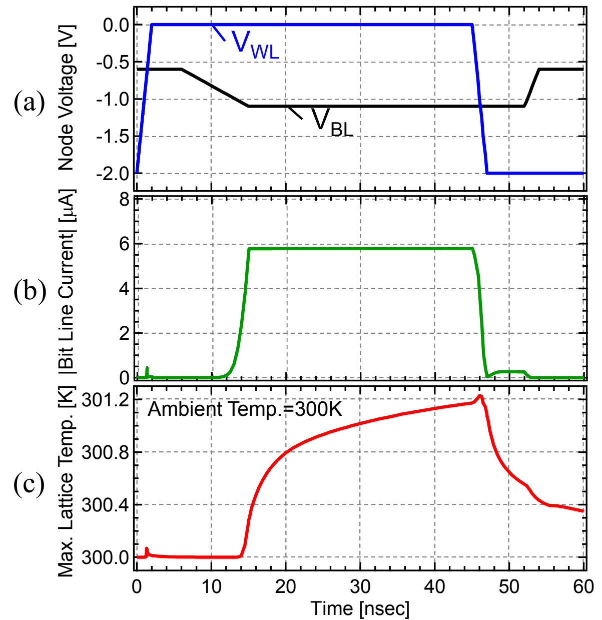

Fig. 3. Write "1" operation of the FED type 1T-DRAM cell. (a) Node voltage (b) Bit line current and (c) Maximum lattice temperature.

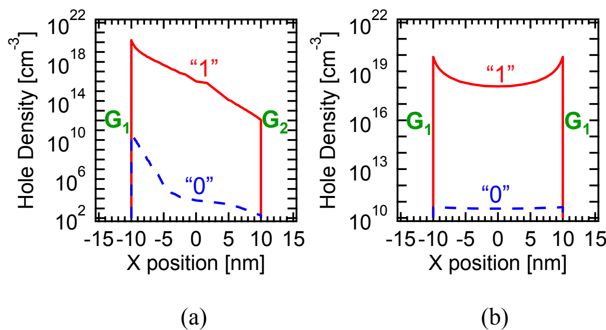

Fig. 4. Distribution of hole density along the channel direction. (a) STL type and (b) FED type.

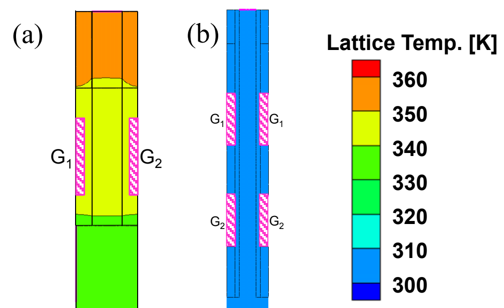

Fig. 5. Distribution of lattice temperature after write "1" operation (time=60nsec). (a) STL type and (b) FED type.