3D Monte Carlo Simulation of III-V Implant-Free Quantum-Well and FinFET MOSFETs

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INTRODUCTION

Following the 2011 edition of the International Roadmap for Semiconductors (ITRS), the III-V/Ge CMOS technology has moved from the "Emerging Materials Devices" areas to the "Process, Integration and Devices" and "Front End Process" areas of the ITRS, which strongly implies that this technology could be utilized at and beyond the 10nm technology node [1]. To extract the greatest benefit from III-V materials, various new transistor architectures have been considered including the Implant-Free Quantum-Well (IFQW) structure and the multi-gate FinFET structure [2]-[4]. In this work we compare the performance of these two III-V nMOSFET architectures designed for the 10nm CMOS technology generation employing $In_{0.53}Ga_{0.47}As$ as the channel material with a high-κ Al_2O_3 gate oxide and a metal gate.

DEVICES AND METHODOLOGY

For the purpose of this work the transistors have been designed to have similar structural details. The structure of the n-type IFQW MOSFET is illustrated in Fig. 1 and the n-type FinFET in Fig. 2. The MOSFET dimensions and doping for the transistors are given in Tables 1-2. Both have an Al_2O_3 gate oxide with a Si_3N_4 lateral spacer. The source and drain regions are epitaxial, in-situ doped raised $In_{0.53}Ga_{0.47}As$, the channel is $In_{0.53}Ga_{0.47}As$ and the substrate is lattice matched $In_{0.52}Al_{0.48}As$. The IFQW transistor has a channel of thickness t_{chn}= 3.75nm and the FinFET has a fin width of W_{fin}= 10nm, and height H_{fin}= 25nm. The channel width of the IFQW is 15nm, and for the FinFET it is $W_{fin}+2\times H_{fin}$= 60nm. Both transistors also include the diffusion of dopants from the source/drain regions into the channel layer [5], which is referred to as sub-diffusion.

The 3D MC module of GARAND [6] is used in this study and provides accurate physical treatment of the non-equilibrium transport in short channel transistors. The MC simulator uses an analytical ellipsoidal, non-parabolic description of the band structure for the III-V materials. Carrier statistics are evaluated using a fully degenerate Fermi-Dirac model that includes the Pauli-Exclusion Principle. Quantum corrections are implemented using a density-gradient approach, which has been calibrated for these devices against a 1D Poisson-Schrodinger solver. The MC module employs the typical scattering mechanisms in III-V materials and the scattering parameters have been calibrated to match the experimentally measured velocity-field and bulk mobility characteristics (Figs. 3-4).

RESULTS

The I_D-V_G characteristics for the two devices are given in Fig. 5 and shows the relationship of drive current per unit width between device architectures. We can report the SS is vastly improved from 88mV/decade in the IFQW to 68mV/dec in the FinFET, and DIBL improves from 85mV/V to 29mV/V. Fig. 6 presents the electron sheet density (per unit width) and velocity of the device with the FinFET having increased electron density in the channel but lower electron velocity. Due to the low DOS of InGaAs, the larger electron density in the FinFET channel increases the impact of degeneracy and forces the electrons into the heavier effective mass L-valleys (see Fig. 7). To conclude, the FinFET structure offers a large improvement in electrostatic control but at higher gate bias doesn't offer improved drive current.

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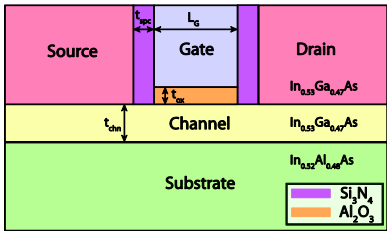

Fig. 1. Device structure of the III-V n-type Implant-Free Quantum-Well MOSFET.

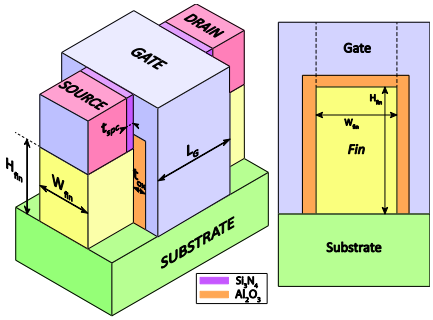

Fig. 2. Device structure of the III-V n-type FinFET MOSFET.

Table 1: IFQW and FinFET structure dimensions.

L_G [nm]	EOT [nm]	T_{ox} [nm]	t_{spc} [nm]
15	0.51	1.125	2

Table 2: IFQW and FinFET doping concentrations.

Src/Drn [cm^{-3}]	Chn. [cm^{-3}]	Subs. [cm^{-3}]
9.1×10^{19}	1.82×10^{17}	3.65×10^{18}

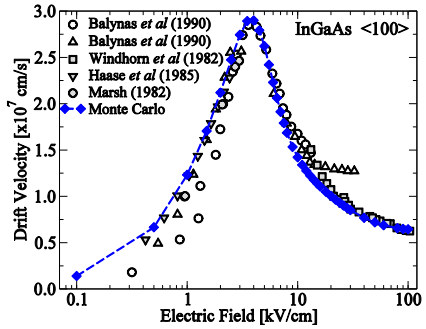

Fig. 3. Calibrated velocity-field characteristic from Monte Carlo simulation for $In_{0.53}Ga_{0.47}As$.

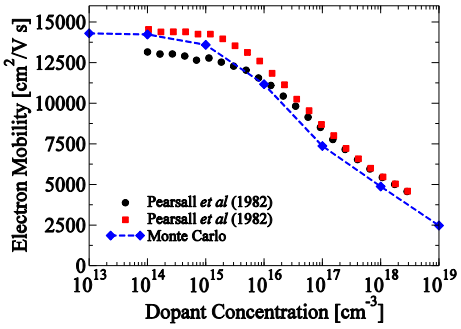

Fig. 4. Calibrated bulk mobility from Monte Carlo simulation for $In_{0.53}Ga_{0.47}As$.

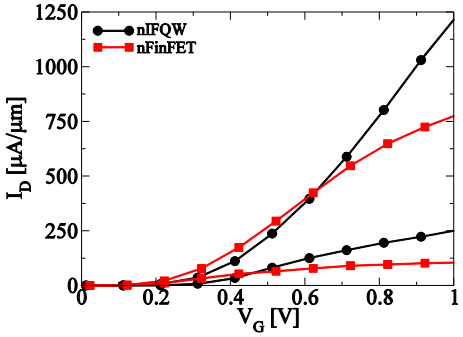

Fig. 5. I_D-V_G characteristics of the III-V nMOSFETs for I_{OFF}= 0.1μA/μm.

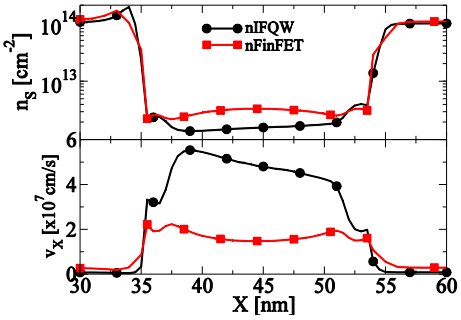

Fig. 6. Sheet density and carrier velocity at V_G=V_D=1V.

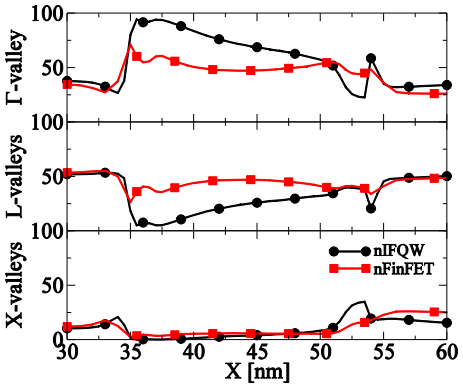

Fig. 7. Conduction band valley occupation [%] at V_G=V_D=1V.