The Monte Carlo approach for investigating electrothermal effects in nanostructures

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INTRODUCTION

Device miniaturization has continued to revolutionize the semiconductor industry for decades. Shrinking device dimensions allowed cramming more components onto integrated circuits (ICs), giving rise to an increased functionality of electronic products. Considering the reported miniaturization trends, as described e.g. by Moore's law [1], the continuous increase in the packing density of ICs have also been followed by an exponential increase in on-chip heat generation. In fact, and for many years, it has been suggested that such trends may not be sustained without significant improvements in cooling technology or fundamental changes in device designs, as unrealistic power density levels and temperatures were predicted. Hot-spots, the low thermal conductivity in thin films and nanowires, and the thermal resistance at interfaces, are but few examples of the difficult challenges faced in guaranteeing the operation of next-generation nanodevices with minimized self-heating. Therefore, for future technology developments, a fundamental understanding of thermal transport at the nanoscale is a necessity. In this context, the development of reliable simulation methods for coupled electron and phonon transport is essential to address all these issues.

SIMULATION METHOD

The simulation work presented here relies on a very well-established Monte Carlo (MC) simulator accounting for self-heating using phonon statistics [2]. The electrothermal simulator self-consistently couples a three-dimensional (3D) electronic trajectory (MC) simulation with the solution of the heat diffusion equation. The Monte Carlo method is very suitable for the simulation of electron transport in semiconductor nanodevices, as it is free from low-field near-equilibrium approximations. More importantly, the method is well-suited for electrothermal modeling, since it allows a detailed microscopic description of electron-phonon scattering. This feature provides an inherent and direct prediction of the spatial distribution of heat generation.

SIMULATION WORK, RESULTS AND DISCUSSIONS

The simulator is employed to study the electrothermal phenomenon in a variety of nanodevices, ranging from conventional Si- and III-V-based field-effect transistors (FETs) to nanowire FET devices. The advantages of using the simulation method are demonstrated. These include: (i) the accurate determination of the spatial heat generation distribution, (ii) the possibility of studying the contribution of the individual phonon populations to heat generation, and (iii) the possibility of accurately studying the effect of self-heating on the microscopic properties of electron transport [3]. The microscopic analysis of self-heating provides a direct means of understanding device electronic and thermal properties, e.g. thermal management and charge confinement in low-dimensional structures. As an example, Figs. 1 and 2 demonstrate a comparison of the electrothermal performance of three mainstream heterostructure devices, including submicron Si, III-As and III-N HEMTs [3]. Fig. 1 shows the variation of the local peak temperature with the input power. From Fig. 1, it can be concluded that GaN HEMTs give the best thermal performance because of the high thermal conductivity of the SiC substrate used in this case. SiGe HEMTs provide the poorest thermal performance mainly due to the very low thermal conductivity of SiGe alloys. Fig. 2 shows the variation of the current reduction due to self-heating with

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the maximum reduction in the electron velocity in the channel. Since the slope of each curve is directly proportional to the 2DEG concentration, this parameter reflects the extent of charge confinement in each device. Fig. 2 indicates how GaN HEMTs provide the best confinement, mainly due to the presence of polarization effects near the channel. Further results will be reported from the simulation of the electrothermal behavior of advanced structures, such as metal-insulator-semiconductor FETs (MISFETs) with a single InAs nanowire channel. In spite of a low average heat dissipation (few orders of magnitude lower than in conventional HEMTs), simulations predict significant local temperatures due to the high current density levels and the poor thermal management in these nanowire structures.

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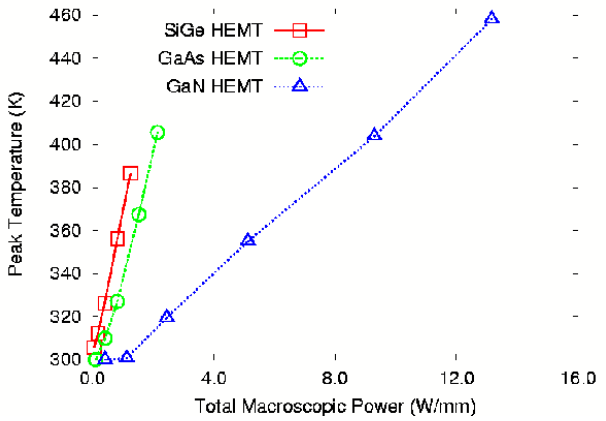

Fig. 1. Variation of the peak temperature with the macroscopic power dissipation for submicron SiGe, GaAs and GaN HEMTs, with a gate length of 200 nm [3].

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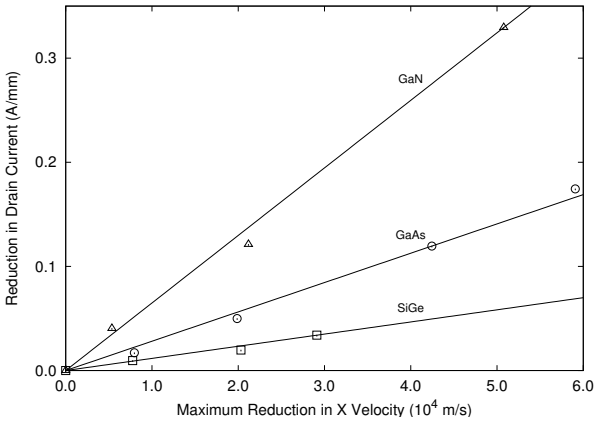

Fig. 2. Variation of the electrothermal reduction in the drain current with the electrothermal reduction in the peak x velocity in the channel for submicron SiGe, GaAs and GaN HEMTs, with a gate length of 200 nm [3].

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