Negative Bias Temperature Instabilities: A Multiscale Approach from First Principles to TCAD Time-Dependent Variability Simulations

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Introduction: Oxide aging and in particular Negative Bias Temperature Instabilities (NBTI) is one of the major threats for device reliability [1]. All traps related effects are now considered as a time-dependent variability, drastically impacting design margins [2, 3]. A robust design aiming oxide reliability impacts reduction relies on a better understanding of the traps properties and, in turn, of their dynamics and their impact on devices, including their interaction with the statistical variability (SV) induced by the atomistic nature of dopants [4]. In this work we present for the first time a unified simulation framework from first principles simulation to TCAD statistical simulations of the time-dependent impact of NBTI on device performances. Defect properties obtained by full oxide processing first principles simulations are used as an input in a drift diffusion simulator, including a physics-based trapping/detrapping model in presence of SV. Existing compact model extraction tools [5] can easily extend these results to the ultimate multiscale simulation tool, from first principles to circuit simulations.

Simulation methodology: Realistic Si/SiO_2 interface models, each of which containing 408 atoms, with 3 nm thick SiO_2 and 3 nm thick Si substrate, were generated by performing molecular dynamics simulations with a proper annealing procedure [6] using the ReaxFF force field [7]. Atomic positions were further refined at density functional theory level using the HSE functional [8]. A prototype defect, i.e. three-coordinated silicon atom in the oxide region dubbed as neutral E' centre, as shown in Figure 1, was identified in the resulting structures as a possible candidate for being responsible of interface traps related effects such as BTI degradation. A uniform distribution, given in Figure 2, of the trap levels associated with this defect in its 0/+ states were determined by shifting its positions, thus demonstrating the impact of the chemical environment on the defect properties. The 0 to + state transition occurs by capturing a hole and switches back when capturing an electron, the latter event being modelled by a simpler model of hole emission, as illustrated in Figure 2. Note that the ++ state features an important reaction energy barrier, leading to much longer term oxide degradation and is not considered in this work.

The defects are implemented in an oxide reliability module on top of GSS quantum corrected, drift diffusion simulator GARAND [9], designed for statistical simulations of SV impact on devices performances. A random position (x_T,y_T) is assigned to each trap, the trap depth into the oxide being fixed at 0.3nm to emulate interface defects. A random energy E_T, uniformly distributed in the obtained trap level range is assigned to each trap. The traps are initially in neutral state 0, after solving the device electrostatic and the current continuity equation, the average hole capture times $<\tau_c>$ are computed for each traps, considering the tunnelling current reaching the trap over the trap cross-section area $\sigma_T=10^{-14}$ cm^2 [10]. Averages hole emission times $<\tau_e>$ are evaluated to respect the SRH balance [11]. Those average values feed a Kinetic Monte-Carlo engine, which randomly chooses the next trap to be charged/discharged and randomly extracts the simulation time step, following an exponential distribution of average value $<\tau_c>$ and $<\tau_e>$ and then reproducing the stochastic character of trapping phenomena. The corresponding charge is assigned in the oxide area using a cloud-in-cell technic and the loop is repeated until the stopping condition has been reached, as shown in the flowchart in Figure 3.

NBTI analysis: 3D simulations of a well-scaled 25nm PMOS device were performed at operating voltages; Figure 4 already shows that these realistic traps will charge at high gate bias and discharge at low gate bias. Figures 5 and 6 give time constants distributions of simulated traps; without/with SV induced by Random Dopants Fluctuations (RDF) and Metal Gate Granularity (MGG); an additional source of variability is induced by trap levels distributions. Figure 7 presents BTI charge traces with/without variability and Figure 8 gives threshold voltage shifts ΔV_T for a single occupied trap and after 0.1 s. of simulated stress for devices with an average trap density of 10^{12} cm^{-2}. The average dynamic impact on V_T is higher for devices with SV but traps are slower on average; dispersions are much higher when variability is considered.

Conclusions: We have presented a multiscale oxide reliability simulation methodology, starting from molecular simulation up to device level large ensemble simulations, demonstrating the SV/trap variability to be determinant both in defects dynamics and impacts.

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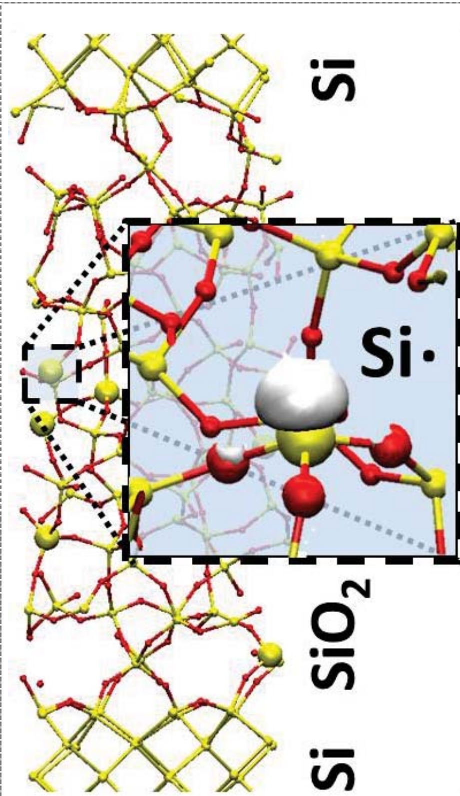

Fig.1 E' centre at the Si/SiO_2 interface, obtained by first principle simulations of oxide melting and annealing. The '+' state presents one hole and one electron localized on the Si_{3C}, one electron delocalizes in the Si conduction band (CB). The chemical environment of the defect impacts the defect energy level.

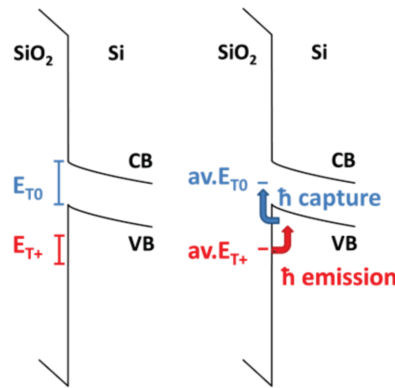

Fig.2 Traps level ranges from first principle simulations in both states E_{T0} ε [3.27, 4.39], E_{T+} ε [5.19, 5.91], (eV, from SiO_2 Cond. band).

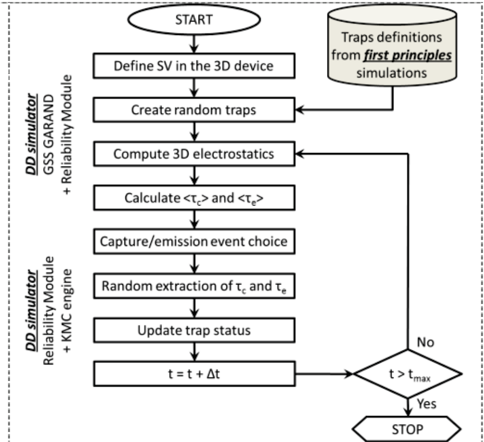

Fig.3 Flowchart of dynamic simulation of time-dependent variability, including first principles inputs.

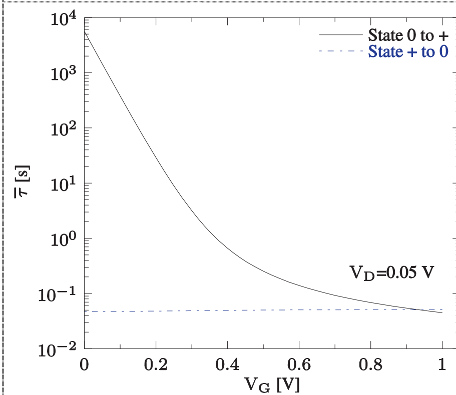

Fig.4 Transition time from a state to another as a function of the gate voltage; in this model holes emission are considered instead of electron capture.

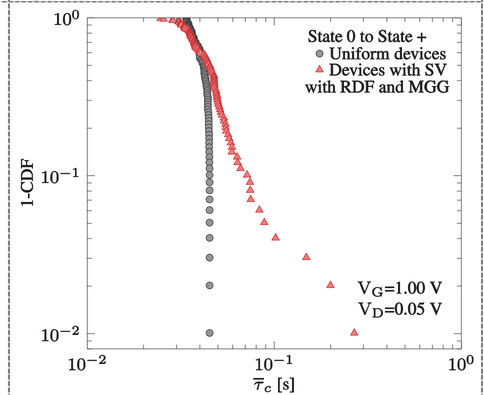

Fig.5 Hole capture time distribution, switching the state from 0 to +. Devices with SV feature RDF and MGG whereas only the trap position is random in uniform devices.

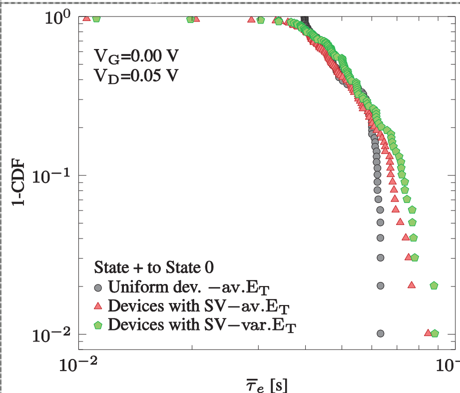

Fig.6 Hole emission time distribution, switching the state from + to 0; in uniform and SV devices with average trap levels; in SV devices with distributed trap levels to account for chemical environment impact.

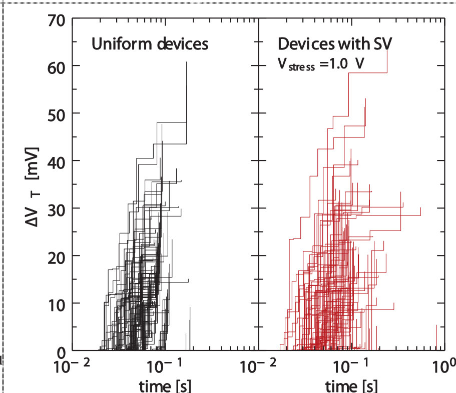

Fig.7 BTI charge traces for uniform devices and devices with SV including a poissonian distributed number of traps with an average of 4; only trapping is considered in this figure, to avoid heavy traces from RTN behaviour.

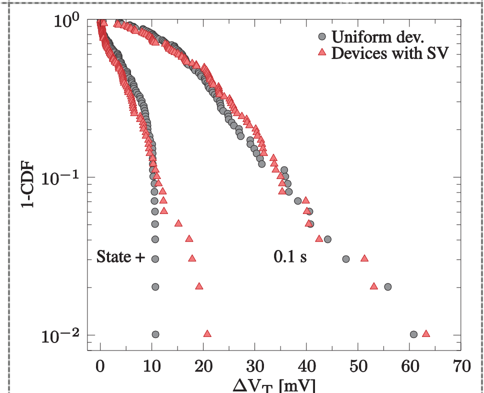

Fig.8 ΔV_T distributions induced by one single charged defect in its + state and extracted distributions after 10^2 s. of stress for uniform and devices with SV.

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