Impact of dielectric induced dynamical many-body correlation effects on the transfer characteristic of Si Nanowire transistor

A. Martinez, J. R. Barker*, and M. Aldegunde
College of Engineering, Swansea University, Singleton Park SA2 8PP
Swansea, UK
*School of Engineering, University of Glasgow, Glasgow G12 8LT, UK
e-mail: a.e.martinez@swansea.ac.uk

Quantum transport has become an essential tool for the TCAD community, as electron confinement and tunneling are important for designing and predicting nanometre devices. The inclusion of phonon scattering for relative large nanotransistor structures is still very time consuming. Futhermore, the efficient incorporation of many body effects such as exchange and correlation into the TCAD simulation remains in progress [1,2]. One of the effects, which becomes important in small structures, is the so-called dielectric confinement [3]. In the case of open systems this effect is not included in the self-consistent Hartree-Fock potential and needs to be added to the self-energy of the electron in the one particle Schrödinger equation. Ref. 1 calculated the effect of this self-energy for different nanowire transistor cross sections. However, the numerical calculation of the self-energy is very time consuming, as it is required for every point in the nanowire.

In this work, we have derived analytical formulae for the calculation of the space-dependent electrostatic self-energy for cylindrical nanowire transistors using an exact Fourier-Bessel analysis that is adapted to square nanowires. The effect of the self-energy in the I_D-V_G characteristic of Si gate-all-around nanowire transistors is studied for different oxide thickness. Two cross-sections (2.2x2.2 nm^2, 3.6x3.6 nm^2) have been considered and two different oxide thickness (0.8, 1.2 nm). Ballistic and dissipative (including phonon scatterings) [4] Non-Equilibrium Green Function simulations for a nanowire transistor with 14/10/14 nm for source/gate/drain are carried out. Fig. 1 shows the self-energy for the 2.2x2.2 nm^2 cross-section and 1.2 nm oxide thickness calculated in one of the planes at the middle of the cross section and perpendicular to one of the confinement direction. There is a substantial downshift (~ 0.1 eV) of the self-energy in the gate relative to the source self energy. This downshift is exhibited in Fig. 2, where the conduction band profile is consequently shifted up to 0.1 eV downwards by the correction. Similarly, in Fig. 2, there is an energy shift downward in source and drain relative to the case without self-energy. This is due to the dielectric confinement and the Neumann boundary condition in source and drain. The corresponding ballistic and dissipative I_D-V_G characteristics are plotted in fig 3. Fig. 4 shows the I_D-V_G characteristics for the 2.2x2.2 nm^2 cross-section and 0.8 nm oxide thickness. Fig. 5 shows the $(I_{DS}-I_D)/I_{DS}$ ratio for ballistic and dissipative simulations. I_{DS} (I_D) denotes the drain current with (without) self-energy included. Fig. 6 shows the corresponding ballistic I_D-V_G for the 3.6x3.6 nm^2 nanowire transistors. In general, the inclusion of the self-energy increases the off current several orders of magnitude for both cross sections and the on current eight times for the small cross section and two times for the large cross section. The effect diminishes rapidly with thicker oxides and wider cross sections. The increase of current due to the electrostatic self-energy correction is smaller when phonon scattering is considered.

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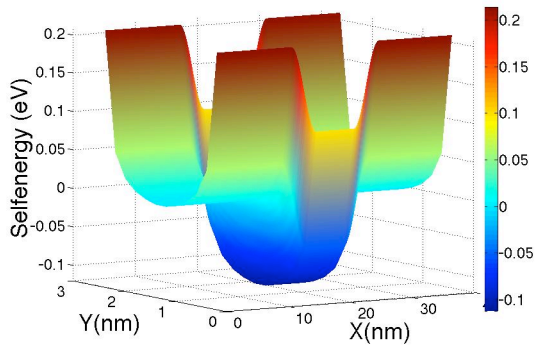

Fig. 1. Self-energy for the 2.2x2.2 nm^2 with 0.8 oxide thickness

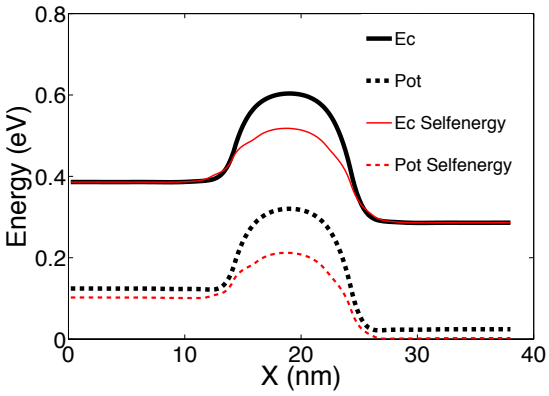

Fig. 2. Conduction band and electrostatic potential energy at Vg=0.6 V for the case of Fig. 1 showing self-energy effects.

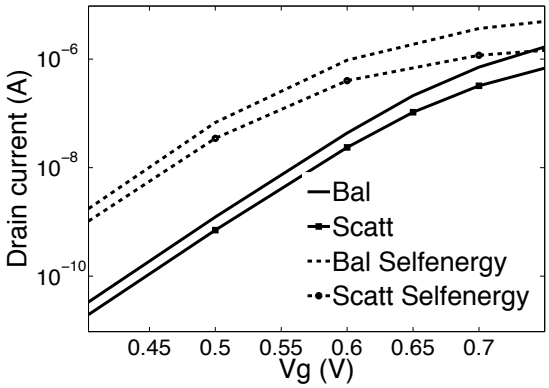

Fig. 3. I_D-V_G for the 2.2x2.2 nm^2 cross section and 1.2 nm oxide thickness device. Dissipative simulations are shown with symbols.

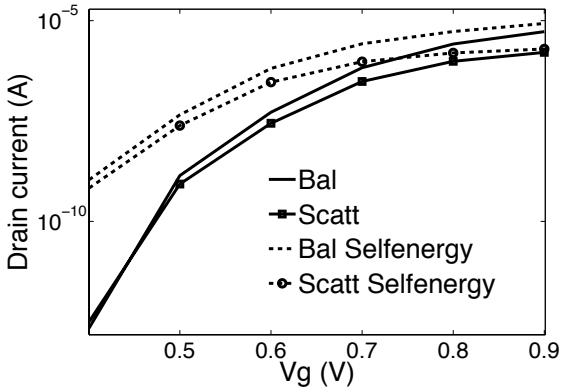

Fig. 4. I_D-V_G for the 2.2x2.2 nm^2 cross-section and 1.2 nm oxide thickness device. Dissipative simulations are shown with symbols.

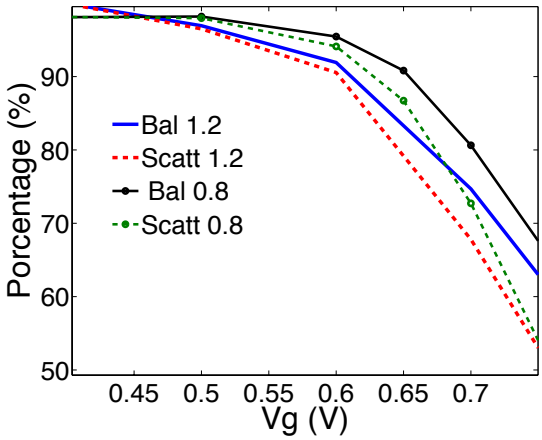

Fig. 5. Drain current increase due to the renormalization of the electron energy. The ballistic and dissipative simulations are shown for the 1.2 and 0.8 oxide thickness cases

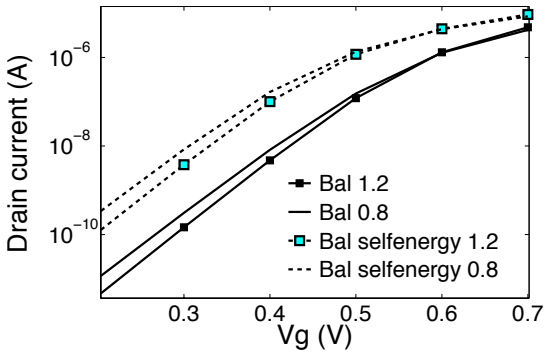

Fig. 6. I_D-V_G for the 3.6x3.6 nm^2 cross-section device.