Self-Heating and Current Degradation in 25 nm FD SOI Devices with (100) and (110) Crystallographic Orientation

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Abstract: ***In this paper we present simulation results obtained with our electro-thermal particle-based device simulator for 25 nm fully depleted silicon-on-insulator devices with (100) and (110) crystallographic orientations. We also investigate the importance of the proper choice of the thermal conductivity model (which is particularly important for thin silicon films) in properly predicting the average maximum temperature and the maximum temperature in the hot spot which are important parameters regarding device reliability.***

Keywords: electro-thermal particle based device simulation, Silicon-On-Insulator devices, thermal conductivity, crystallographic orientations.

I. INTRODUCTION

Over the last four decades silicon CMOS technology has emerged as the predominant technology of the microelectronic industry. The concept of device scaling has been applied over many technology generations resulting in consistent improvements in both device density and performance [1]. As channel lengths shrink bellow 30 nm, complex channel profiles are required to achieve the desired threshold voltages and to alleviate short-channel effects. At such reduced gate-length, the challenge is to maintain the high drive current with low leakage while controlling short-channel effects.

The current trend in device scaling is a transition away from conventional planar CMOS to alternative non-planar technology devices, such as fully-depleted (FD), dual-gate (DG), tri-gate silicon-on-insulator (SOI) and other transistor types [2]. The advantages of these SOI devices are higher drive current, low junction capacitance, reduced leakage current, suppression of floating-body effects, absence of latch-up and ease in scaling.

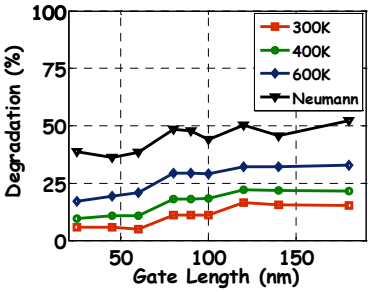

Figure 1. Current degradation vs. technology generation ranging from 25 nm to 180 nm channel length FD SOI devices. Isothermal boundary condition of 300K is set on the bottom of the BOX. Parameter is the temperature on the gate electrode. Neumann boundary conditions are applied at the vertical sides.

But, one of the major problem with SOI devices is that they exhibit self-heating effects. These effects arise from the fact that the underlying SiO_2 layer has about 100 times smaller thermal conductivity than bulk Si (1.4 W/m/K). Also, the thickness of the silicon film in nanoscale devices is much smaller than the phonon mean free path which is on the order of 300 nm in bulk silicon. Therefore, boundary scattering becomes dominant scattering mechanism [3], [4] thus reducing the thermal conductivity value to a fraction of its bulk value. For example, the bulk thermal conductivity in silicon is 148 W/m/K and the thermal conductivity of a silicon film of thickness of 10 nm is 13W/m/K (a factor of 10 smaller than the bulk value). Also, in thin silicon films the thermal conductivity has smaller temperature dependence because boundary scattering is temperature independent scattering process.

To address the problem of lattice heating in nanoscale silicon-on-insulator (SOI) devices in a more rigorous manner from what exists in the literature, we have developed a thermal particle-based device simulator that self-consistently solves the steady-state Boltzmann transport equation (BTE) for the electrons and the energy balance equations for the acoustic and optical phonons. The simulator [5], [6] has been used in investigation of self-heating effects in different technology nodes of nanoscale FD-SOI devices and dual gate device structures. Our simulation results suggest that self-heating has less degrading effect on the on-current in smaller devices in which non-stationary transport and velocity overshoot effect dominate the carrier transport.

In the two sections that follow we first discuss the importance of proper choice of the thermal conductivity model for proper determination of the temperature of the hotspot (Section II). In Section III, we describe self-heating effects and current degradation in 25 nm FD SOI devices with several different transport directions. Conclusions related to this research are given in Section IV.

II. Temperature and Thickness Dependent Thermal Conductivity Model

In the past, the electro-thermal device simulator has been used in the examination of heating effects in different generations of fully depleted (FD) nanoscale SOI devices. In those analyses we have assumed that the thermal conductivity of the Si layer was temperature independent and characterized by a fixed value of 13 W/m/K that corresponds to a value for 10-nm thick silicon film. In a more recent work, to derive more realistic estimates of the current degradation, we proposed a new theoretical model for the temperature and thickness dependent thermal conductivity based on the work of Sondheimer [7]. Namely, the thermal conductivity of a semiconductor film of a thickness a, under the assumption that the z-axis is perpendicular to the plane of the film, the surfaces of the film being at z=0 and z=a, is given by:

$$\kappa(z)=\kappa_0(T)\int_0^{\pi/2}\sin^3\theta\left\{1-\exp\left(-\frac{a}{2\lambda(T)\cos\theta}\right)\cosh\left(\frac{a-2z}{2\lambda(T)\cos\theta}\right)\right\}d\theta \quad (1)$$

where $\lambda(T)$ is the mean free path expressed as $\lambda(T)=\lambda_0(300/T)$ (T in K) where room temperature mean free path of bulk phonons is taken to be λ_0=290 nm.

Selberherr [8] has parametrized the temperature dependence of the bulk thermal conductivity in the temperature range between 250K and 1000K. In our case we find that the appropriate expression is:

$$\kappa_0(T)=\frac{135}{a+bT+cT^2}\quad \text{W/m/K} \quad (2)$$

where a=0.03, b=1.56×10^{-3}, and c=1.65×10^{-6}. Eqs. (1) and (2) give almost perfect fit to the experimental and the theoretical data reported in an Asheghi paper [4] (see Figure. 2).

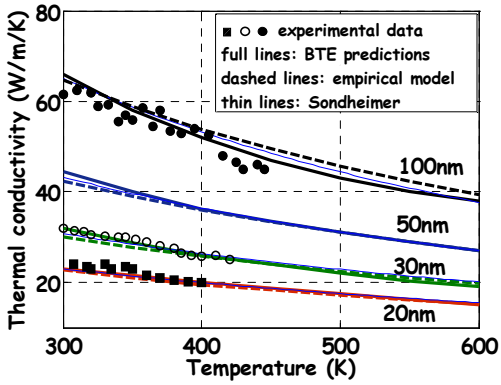

Figure 2. Silicon film thickness dependence of the average thermal conductivity at T=300 K vs. active silicon layer thickness. Experimental data are taken from the work of Asheghi and co-workers [4].

In the actual implementation of the model in the code, we have modified the expressions provided by Dutton and co-workers [9] to include the temperature dependence of the mean free path as it is done in Eq. (1). The empirical model data together with the experimental data, the Monte Carlo simulations and the Sondheimer model with the temperature dependent mean-free path are all shown in Figure 2. We see that the empirical model is very close to the Sondheimer model. Simulation results for different generations of nanoscale FD-SOI devices showed that it is important what model is used in the simulation for the thermal conductivity in properly predicting the average maximum temperature in the hot spot of the device (see Figure 3).

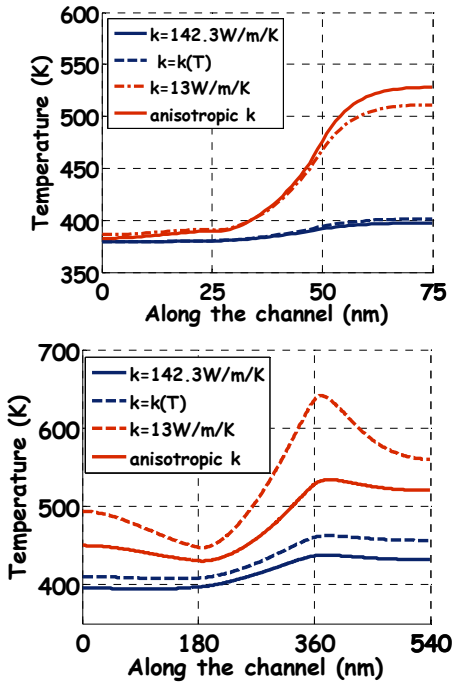

Figure 3. Average lattice temperature profile in the active Si-layer for a 25 nm gate length (top) and a 180 nm gate length (bottom) FD SOI MOSFET, using different thermal conductivity models (1-bulk thermal conductivity model, 2-temperature-dependent bulk thermal conductivity model, 3-fixed thermal conductivity value of 13W/m/K corresponding to a silicon film of 10 nm at 300 K, 4-anisotropic thickness and temperature dependent thermal conductivity).

III. Inclusion of Thermal Conductivity Tensor for Arbitrary Crystallographic Orientations

In this work, we further extend our investigations on the current degradation in nanoscale FD-SOI devices due to self-heating effects. Here, the focus is on the inclusion of the thermal conductivity tensors as calculated by Aksamija and co-workers [10] using a full-band structure model for the phonon dispersions (see Figure 4). The anisotropy of the effective mass for different crystallographic transport directions has been accounted for using the approach of Rahman and co-workers [11].

In Figures 5 and 6 we present the thermal conductivity profiles in the active Si-layer for 25 nm channel length FD-SOI device for (100) and (110) wafer orientations using our temperature and position dependent thermal conductivity model [12] as compared to the results obtained when using the temperature dependent thermal conductivity tensor model of Aksamija and co-workers [10]. Simulation results show that due to the lower thermal conductivity in the channel region obtained with our model, the lattice temperature in the active Si-layer is higher when compared to the results obtained when using the thermal conductivity tensors model (see Figure 7, bottom panel). Note, that from thermal point of view, (110) wafer orientation gives better results (lower hot spot temperature). However, from electrical point of view, although the current degradation is lower for (110) orientation, the on-current is smaller compared to the value of the (100)-orientation (see Figure 7, top panel).

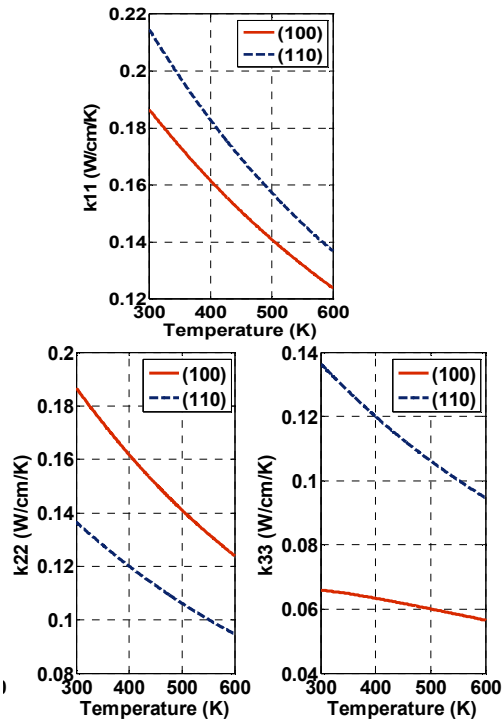

Figure 4. Temperature dependence of diagonal thermal conductivity tensors for (100) and (110) wafer orientations. Off-diagonal elements are very small and can be neglected.

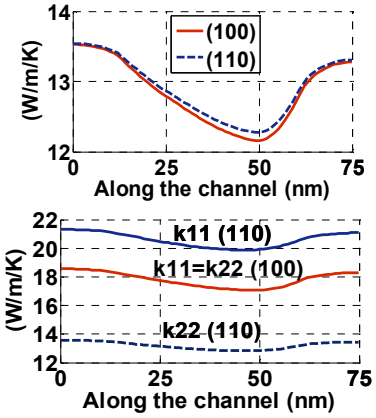

Figure 5. Average thermal conductivity profile profile in the active Si-layer in 25nm channel length FD-SOI for (100) and (110) wafer orientations using: (top: our thermal conductivity model; bottom: thermal conductivity tensors).

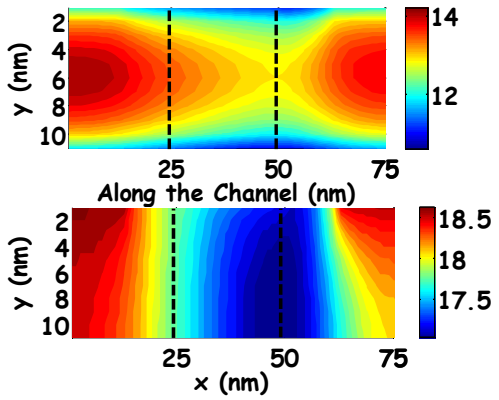

Figure 6. Thermal conductivity profile (in W/m/K) in the active Si-layer in 25nm channel length FD-SOI for (100) wafer orientation (top: using our thermal conductivity model; bottom: using thermal conductivity tensors).

IV. Conclusion

In this paper we have compared self-heating and current degradation for 25 nm FD SOI devices using different transport orientations and different thermal conductivity models. Simulation results show that from thermal point of view (110) device gives better results, but (100) device has higher on-current. Thus, one must make a trade-off between the higher temperature in the hot-spot and the higher on-current value. We also showed that it is important what model is used in the simulation for the thermal conductivity in properly predicting the average maximum temperature in the hot spot of the device.

Wafer orientation	Type of simulation	κ_{th} model	Current (mA/um)	Current Degradation (%)
(100)	isotherm.	/	1.828	\
(100)	thermal	1	1.757	3.88
(100)	thermal	2	1.768	2.28
(110)	isotherm.	/	1.235	\
(110)	thermal	1	1.197	3.08
(110)	thermal	2	1.197	3.08

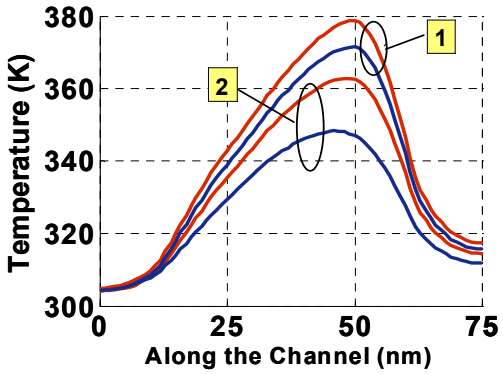

Figure 7. Top panel: Current Degradation for 25 nm FD-SOI and Bottom panel: Average lattice temperature profile in the active Si-layer. (1-our thermal conductivity model; 2-thermal conductivity tensor); red lines –(100) orientation; blue lines – (110) orientation.

ACKNOWLEDGEMENT

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