Monte Carlo simulations of inverse channel versus implant free $In_{0.3}Ga_{0.7}As$ MOSFETs

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***Abstract*—A performance of two n-type III-V MOSFET based on an $In_{0.3}Ga_{0.7}As$ channel architecture: a surface channel design with implanted source/drain contacts and a δ-doped, implant-free design, is compared when scaled to gate lengths of 35 nm, 25 nm and 18 nm. The transistor characteristics are simulated using ensemble heterostructure finite element Monte Carlo device simulations assisted by drift-diffusion simulations in a sub-threshold region. The Monte Carlo simulations include a calibrated quantum corrections for each of the scaled transistor and two interface related scattering mechanisms: interface roughness and interface phonons at the interface of polar-polar materials. The scaling of surface channel MOSFETs delivers an increase in the device on-current despite the negative impact of interface phonons, while the implant free MOSFETs scaled to 18 nm gate length suffer substantially from a largely enhanced scattering due to interface roughness and phonons.**

I. Introduction

The introduction of higher mobility materials such as Ge [1] for p-type MOSFETs and III-Vs [2] for n-type MOSFETs for sub-16 nm technology is an accepted option. A very low electron effective mass in the lowest energy valley of III-V materials assures a very high injection velocity which, in combination with high mobility and low backscattering, promises a very high device performance [3]. However there are factors that could counterbalance this promise. The lower density of states (DOS), inherit to III-V materials, can reduce the performance of scaled transistors due to increased parasitic quantum gate capacitance which necessitates a larger gate overdrive in order to achieve acceptable carrier concentration in the channel. This can also lead to a carrier starvation in the source region limiting the number of carriers supplied to the channel [4]. Electron transfer to higher valleys (with larger electron effective masses) may also restrict the current enhancement depending on where such transfer occurs close to the source or much further along the channel. Will the real **r**-space transfer of carriers through the channel be faster than the **k**-space transfer to upper valleys? Surface channel (SC) III-V MOSFETs might struggle to take advantage of low effective mass and high injection velocity into the channel. Therefore, new device ultra-thin body concepts including an enhancement mode MOSFET with implant free (IF) source/drain regions [3] as well as HEMT structures [5] have been studied.

In this work, we compare the performance of two n-type III-V MOSFET $In_{0.3}Ga_{0.7}As$ channel architectures: (i) the SC design with implanted S/D (Fig. 1) and (ii) the δ-doped IF design (Fig. 2), each scaled to gate lengths of 35, 25 and 18ñm. The scaled 35, 25 and 18ñm gate length SC MOSFETs have S/D extensions n-type doped up to $1, 2$, and $3\times10^{19}\mathrm{cm}^{-3}$ and uniformly p-type doped channel to $5, 7$, and $8\times10^{17}\mathrm{cm}^{-3}$, respectively. The high-κ gate oxide is assumed to be GdGaO (GGO) with $\kappa = 20$. The scaled IF MOSFETs have all the same δ-doping concentration of $3.55\times10^{12}\mathrm{cm}^{-2}$, however, the layer of GaAs spacer (see Fig. 2) is scaled from 3 nm to 2 nm and 1.5 nm. The EOT is kept as close as possible in both SC (1.0 nm, 0.9 nm, and 0.7 nm) and IF (1.5 nm, 1.0 nm, and 0.75 nm) architectures during the scaling process taking into account technological limitations. The doping profiles for the SC transistors are optimized using a drift-diffusion (DD) simulator (MEDICI). Conduction band profile and electron density in SC and IF MOSFETs are shown in Fig. 3, respectively.

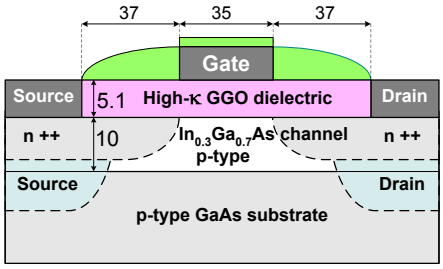


Fig. 1. Cross-section of the 35 nm gate length, n-type, surface channel (SC), $In_{0.3}Ga_{0.7}As$ MOSFET. Dimensions quoted in nm.

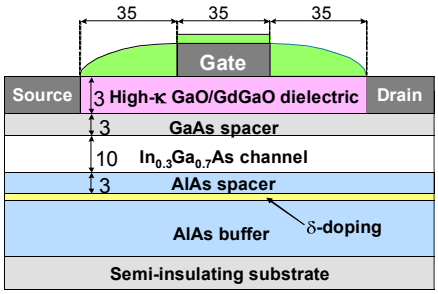
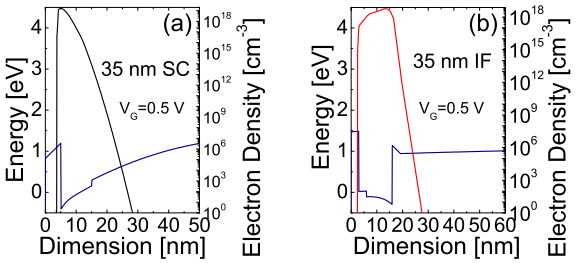


Fig. 2. Cross-section of the 35 nm gate length, implant free (IF) $In_{0.3}Ga_{0.7}As$ MOSFET. Dimensions quoted in nm.



(a) (b)

Fig. 3. Conduction band and electron density in the 35 nm gate length SC (a) and IF (b) MOSFETs.

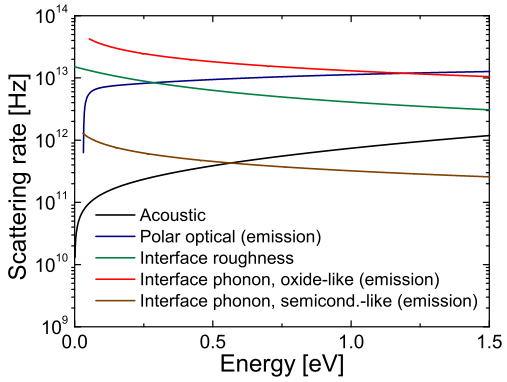


Fig. 4. Electron scattering rates vs. energy in $In_{0.3}Ga_{0.7}As$ channel illustrating a strength of the most operative electron interactions.

II. Surface Channel and Implant Free InGaAs MOSFETs

This study is carried out using a hetero-structure finite element Monte Carlo device simulator MC/MOS [3], [9] assisted by DD simulations. The main goal is to study the on-current including an electron (e) scattering with interface (soft) optical phonons (IP) [7]. The e-IP interaction is derived in a non-parabolic band-structure approximation, by calculating total (high/low frequency, $\epsilon^{\alpha}_{\mathrm{TOT}(\eta)}$ $[\alpha = \infty, 0]$) dielectric functions via solving a biquadratic equation

$$\omega^4\left(\epsilon^{\infty}_{OX}+\epsilon^{\infty}_{PS}\right)-\omega^2\left[\epsilon^{0}_{OX}\left(\omega^{TO}_{OX}\right)^2+\epsilon^{\infty}_{OX}\left(\omega^{TO}_{PS}\right)^2+\right.$$
$$\left.+\epsilon^{0}_{PS}\left(\omega^{TO}_{PS}\right)^2+\epsilon^{\infty}_{PS}\left(\omega^{TO}_{OX}\right)^2\right]+\left(\omega^{TO}_{PS}\right)^2\left(\omega^{TO}_{OX}\right)^2\left(\epsilon^{0}_{OX}+\epsilon^{0}_{PS}\right)$$
$$=0.$$

Gate [nm]	Surface channel		Implant free	
	V_D=0.05 V	V_D=1.0 V	V_D=0.05 V	V_D=1.0 V
	Sub. slope [mV/dec]		Sub. slope [mV/dec]	
35	75	86	94	97
25	82	106	96	101
18	91	132	121	139

TABLE I
Comparison of sub-threshold slopes in the scaled SC and IF $In_{0.3}Ga_{0.7}As$ MOSFETs.

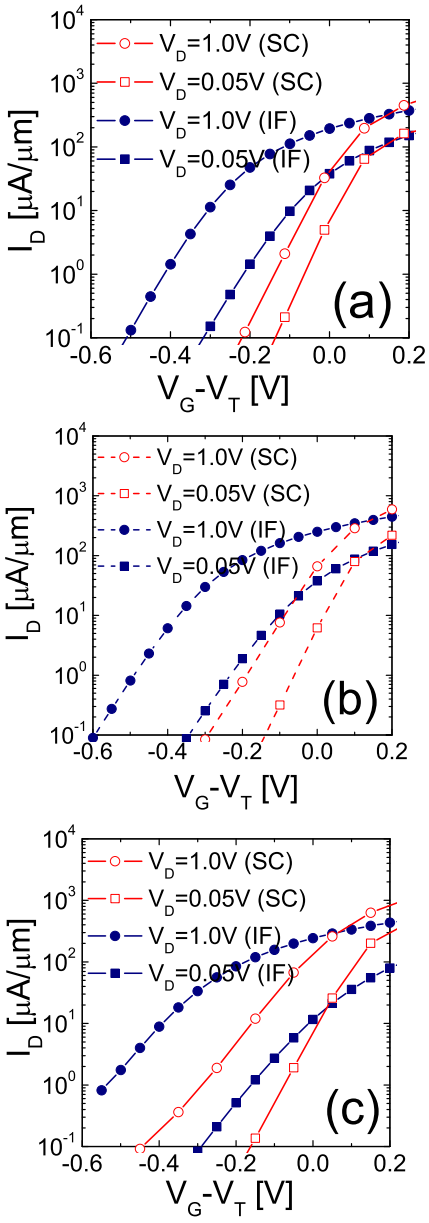


Fig. 5. Sub-threshold slopes at high and low V_D for 35 nm (a), 25 nm (b) and 18 nm (c) gate length SC and IF MOSFETs.

considering the interface between dielectric (OX) and polar semiconductor (PS) which have respective transverse optical (TO) frequencies ω^{TO}. The resulting frequencies ω are then needed for a calculation of the interaction strength. Using the strongest TO phonon in GaO_2 with energy of 35.07 meV [8], we have found two interface TO phonons at the $GaO_2/In_{0.3}Ga_{0.7}As$ interface with energies of 29.85 meV and 52.52 meV, respectively. Figure 4 shows the interaction strengths of the most important scattering mechanisms in the $In_{0.3}Ga_{0.7}As$ channel. In addition, the MC simulations use a non-parabolic anisotropic three-valley bandstructure approximation, and include also impact of the strain in the InGaAs

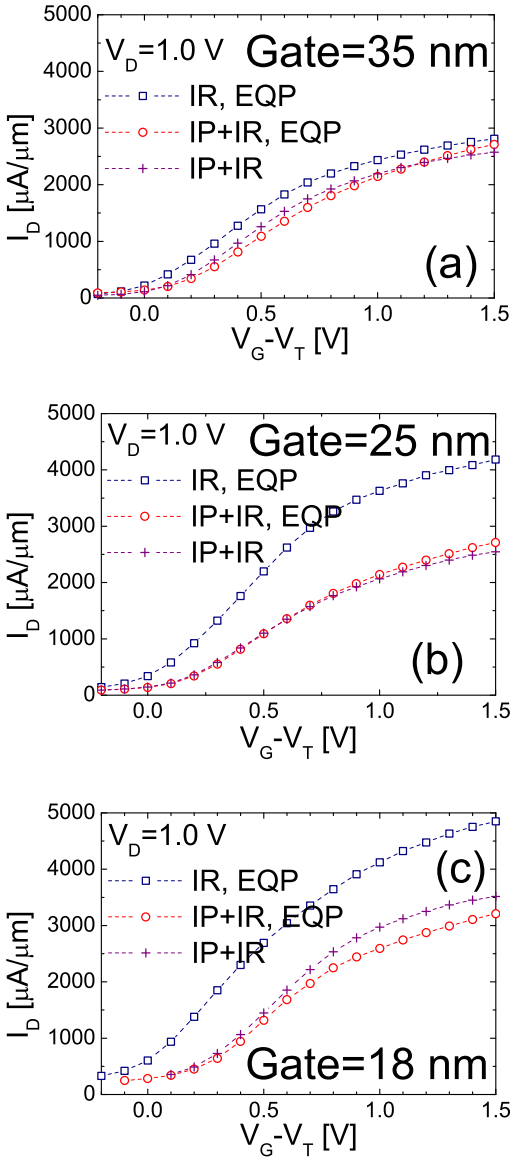


Fig. 6. I_D-V_G characteristics for the (a) 35 nm, (b) 25 nm and (c) 18 nm gate length SC $In_{0.3}Ga_{0.7}As$ MOSFETs at a drain bias of 1.0 V, respectively. The incremental impact of interface roughness (IR), interface phonons (IP), and quantum corrections (EQP) used in MC simulations is also shown. The threshold voltage is adjusted to 0.0 V.

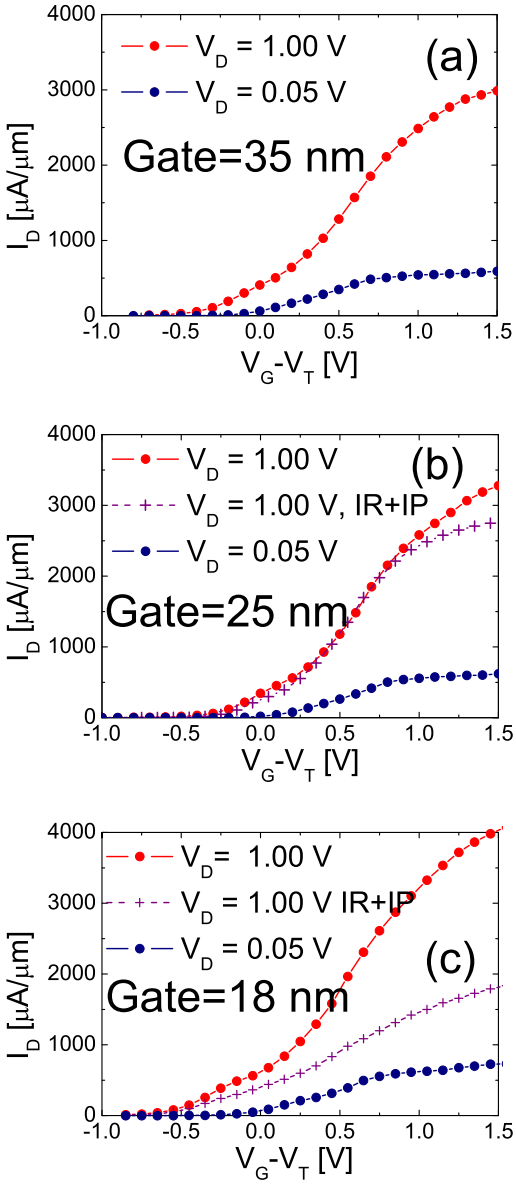


Fig. 7. I_D-V_G characteristics of IF $In_{0.3}Ga_{0.7}As$ channel MOSFET with gate lengths of (a) 35 nm, (b) 25 nm and (c) 18 nm at drain biases of 0.05 V and 1.0 V, respectively, showing the impact of interface roughness (IR) and interface phonons (IP). The quantum corrections (EQP) are always included and V_T is adjusted to 0.0 V.

channel (on bandgap, valley positions, effective masses, polar optical phonon energy and deformation potential) [3]. The ionized impurity scattering is using Fermi-Dirac statistics self-consistently calculating Fermi energy and electron temperature for static screening model [9]. Quantum corrections are included via the effective quantum potential (EQP) method [3].

Figure 5 compares sub-threshold slope of the SC and IF $In_{0.3}Ga_{0.7}As$ MOSFETs when scaled to gate lengths of 35, 25 and 18 nm. The sub-threshold slopes for the scaled SC and IF $In_{0.3}Ga_{0.7}As$ MOSFETs obtained from the DD simulator are summarized in Table I. The sub-threshold slope deteriorates in the scaling process for the both SC and IF MOSFET variants at the similar rate but the slope of IF device architecture substantially deteriorates also at low drain bias of 0.05 V. This is due to a large loss of control of the gate over channel transport in the scaling process of the IF devices compared to the scaling of the SC devices.

Figure 6 shows I_D-V_G characteristics at V_D of 1.0 V for 35, 25, and 18 nm gate length SC MOSFETs, respectively. The performance of equivalent gate length IF MOSFETs is shown in Fig. 7, at the same 1.0 V overdrive. At an overdrive of 1.0 V, this device architecture delivers a drive current of

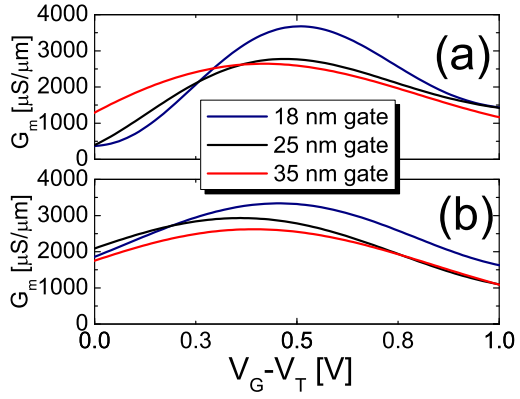


Fig. 8. Transconductance (G) for scaled SC (a) and IF (b) device architectures at $V_D = 1.0$ V.

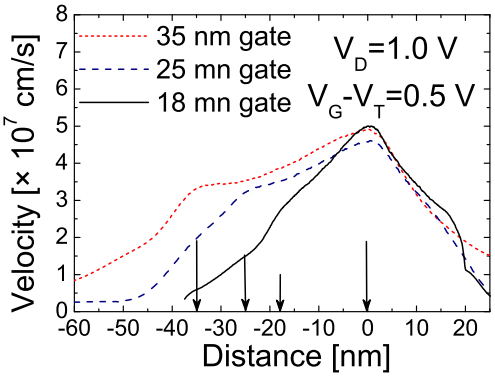


Fig. 9. Average velocity along the $In_{0.3}Ga_{0.7}As$ channel in scaled SC MOSFETs using IP, IR and EQP.

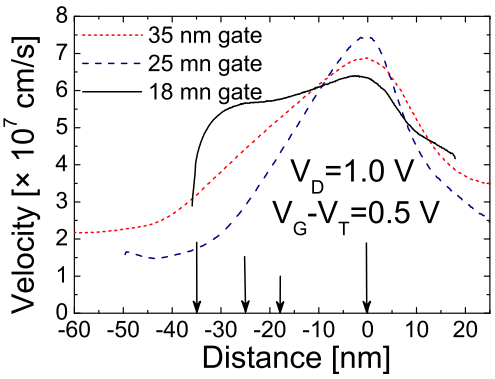


Fig. 10. Average velocity along the $In_{0.3}Ga_{0.7}As$ channel in scaled IF MOSFETs using IP, IR and EQPEQP in simulations.

2260 μA/m for a gate length of 35 nm. This decreases to 2144 μA/m due to a strong impact of the IP scattering for a gate length of 25 nm, and increases to 2594 μA/m for the 18 nm gate length device. The incremental impact of the IP and interface roughness (IR) scattering mechanisms in the channel on the drain current is also presented. On the other hand, the equivalent gate length IF transistors will deliver a drive current of 2475 μA/m, 2480 μA/m and 1496 μA/m at gate lengths of 35 nm, 25 nm and 18 nm, respectively, as shown in Fig. 7, at the same 1.0 V overdrive.

Figure 8 compares transconductance of the scaled SC and IF variants which indicates no improvement in the performance of SC MOSFETs when scaled from a gate length of 35 nm to 25 nm while the IF variant delivers some improvement. The transconductance also clearly reveals that the scaling of SC architecture to 18 nm gate length brings a much large improvement in the performance than the scaling of the IF MOSFET to the same gate length. The corresponding average electron velocity in the scaled SC and IF devices is compared in Figs. 9 and 10, respectively, illustrating a much larger channel velocity in the scaled IF transistors. However, the velocity profile in the 18 nm gate length IF transistor also shows how the maximum peak velocity in the channel declines explaining the dramatic lowering of the on-current [see Fig. 7(c)].

III. Conclusion

In summary, the SC transistor architecture suffers stronger from the IP scattering induced reduction in the on-current when scaled from 35 nm gate length to 25 nm when compared to the IF devices. However, the IF MOSFETs start to suffer from the IP scattering when their gate length is reduced to 18 nm. These observations are highlighted by the calculated transconductance which illustrates a minuscule improvement in the performance of the 25 nm gate length SC MOSFET from the 35 nm gate length and a large jump in the performance when scaled further. It also shows the that the performance of IF architecture is steady but relatively small. The velocity profiles for scaled devices of the both variants can give an insight into this behaviour. The sub-threshold slope of scaled transistors deteriorates similarly in the both SC and IF MOSFETs but the IF architecture suffers also from the additional deterioration of the slope at a low drain bias.

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References

[1] H. Shang K.-L. Lee, P. Kozlowski, C. D'Emic, I. Babich, E. Sikorski, M. Ieong, H.-S. P. Wong, K. Guarini, and W. Haensch, Electron Device Lett., vol. 25, no. 3, pp. 135-137, March 2004.

[2] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic,, IEEE Trans. Nanotechnol., vol. 4, no. 2, pp. 153-158, Mar. 2005.

[3] K. Kalna J. A. Wilson, D. A. J. Moran, R. J. W. Hill, A. R. Long, R. Droopad, M. Passlack, I. G. Thayne, and A. Asenov, IEEE Trans. Nanotechnol., vol. 6, pp. 106-112, Jan. 2007.

[4] M. V. Fischetti and P. O'Regan Terrance, IEEE Trans. Electron. Devices, vol. 54, no. 9, pp. 2116-2136, 2007.

[5] N. Waldron, D.-H. Kim, and J. A. del Alamo, IEDM Tech. Dig., pp. 633-636, 2007.

[6] K. Kalna, L. Yang, and A. Asenov, Proc. ESSDERC, pp. 169-172, 2005.

[7] S. Q. Wang and G. D. Mahan, Phys. Rev., vol. B 6, no. 12, pp. 4517-4524, Dec. 1972.

[8] Y.-M. Chang, L. Xu, and H. W. K. Tom, Phys. Rev., vol. B 59, no. 19, pp. 12220-12223, May 1999.

[9] K. Kalna, L. Yang, and A. Asenov, in Proc. ESSDERC, pp. 169-172, Sept. 2005.